Rev: 080508

DS33Z11 Demo Kit

General Description

The DS33Z11 demo kit is an easy-to-use evaluation board for the DS33Z11 Ethernet transport-over-serial link device. The DS33Z11DK contains an integrated Ethernet PHY and serial link. The serial link is complete with transceiver, transformers, and network connections. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

Demo Kit Contents

DS33Z11DK Main Board
5.0V Wall Adapter
BNC Adapter (2-pin coax)
CD-ROM
- ChipView Software and Manual
- DS33Z11DK Data Sheet
- Configuration Files

Ordering Information

PART	TYPE
DS33Z11DK	DS33Z11 demo kit

Features

- **Demonstrates Key Functions of DS33Z11 Ethernet Transport Chipset**
- **On-Board DS2155 T1E1 SCT, DS3170 T3E3 SCT, Transformers, BNC Adapter, and RJ48 Network Connectors and Termination**
- **Provides Support for Hardware and Software Modes**
- **Device Driver Provides Automatic Configuration for T1, E1, T3, and E3 Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z11, DS2155, and DS3170 Register Sets**
- **All DS33Z11 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**
- **Integrated Power-Supply Interfaces with 5.0V Wall Adapter**

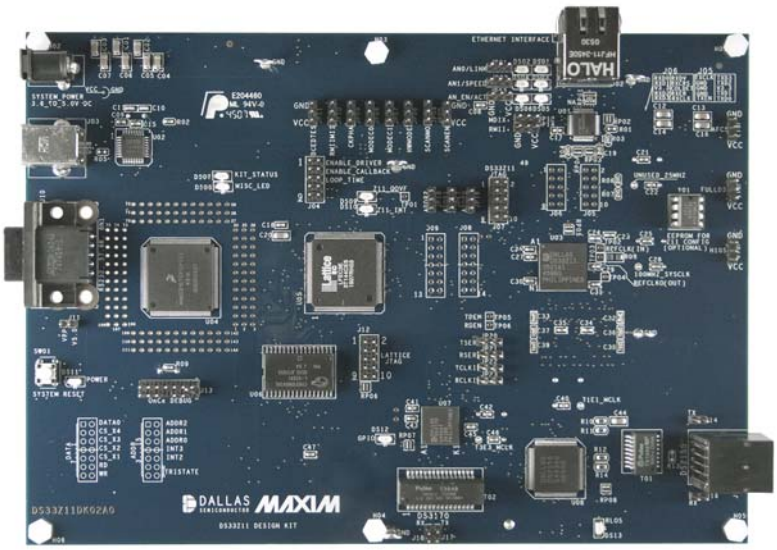
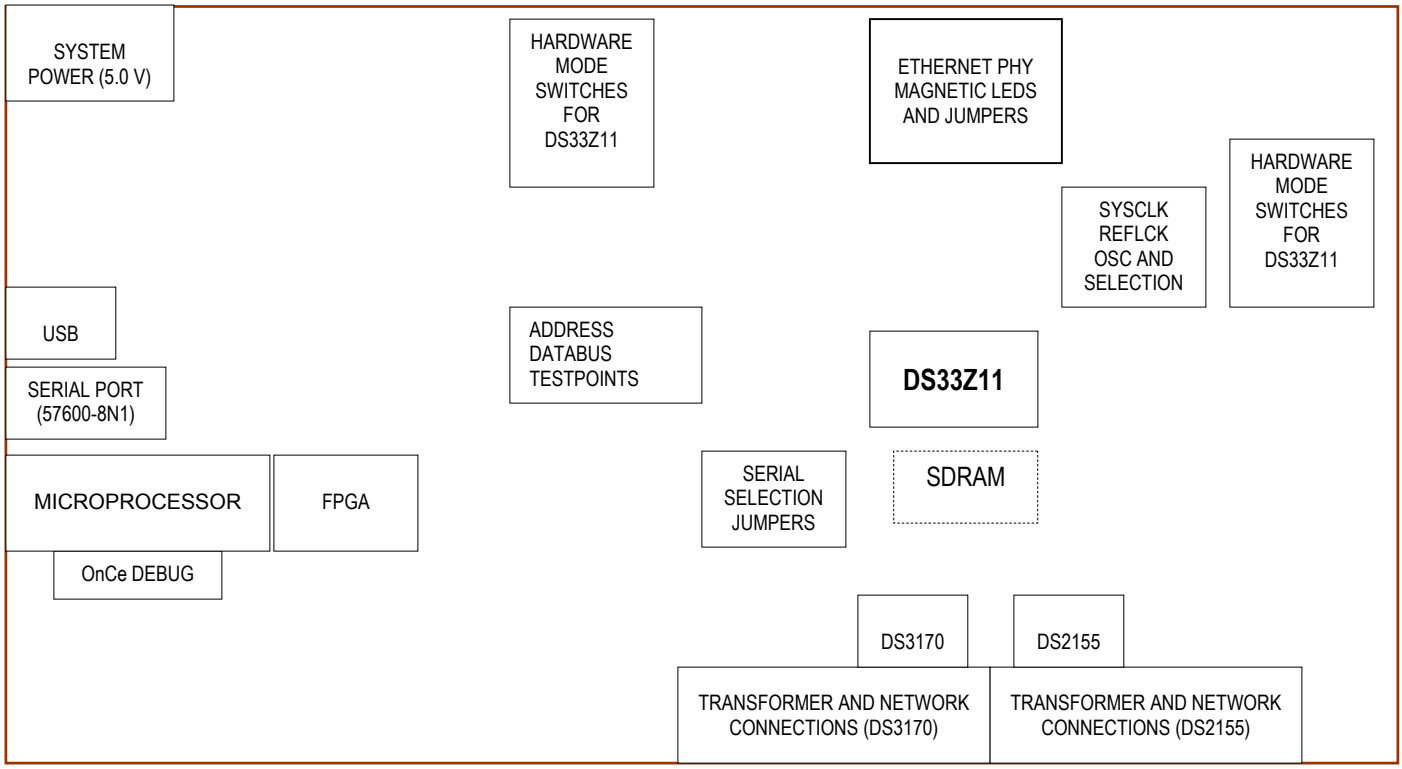


Table of Contents

List of Figures

List of Tables

1. System Floorplan



2. PCB Errata

- The following errata apply to DS33Z11DK02A0:
  - DS33Z11 RSER and TSER wires were crossed. The schematic has been corrected, and PCBs have been reworked to match the schematic.
  - Header J04 pins 1, 3, 5, 7, 9 were not connected to VCC. The schematic has been corrected, and PCBs have been reworked to match the schematic.

3. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

3.1 Powering Up the Demo Kit

- Connect PCB 5.0V wall adapter to the power jack. LED DS11 should light.
- Connect RS232 serial cable, or USB cable between the host PC and demo kit.
- Connect the Ethernet port to an ordinary PC, or network test equipment. Either a patch or crossover cable may be used. The link LED should turn on after connecting the cable.
- Set Jumpers for software mode as described in Table 1 (short description follows).
  - Top bank all GND (DCEDTE ….. SCANEN), with exception for MODEC0 which is at VCC
  - A2, A1, A0 Jumpered to pins 2+3
  - Right Bank all to VCC (AFCS, FULLDS, H1OS)
- Upon power-up, the processor FPGA Status LEDs (DS07 green) will be lit. Interrupt LEDs (DS09 red) will not be lit. DS33Z11 Queue overflow LEDs (DS10 red) will not be lit. PHY LINK LED (DS02/DS01 green) should be lit if the Ethernet is connected.

3.2 Installing and Running the Software

ChipView is a general-purpose program that supports a number of Maxim demo kits. To install the ChipView software, run SETUP.EXE from the disk included in the DS33Z11DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS33Z11DK.

After installation, run the ChipView program with the DS33Z11DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial (or USB) port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Maxim evaluation platforms. In the active subwindow, select the DS33Z11.DEF definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS33Z11 register map. Other definition files may be loaded, and navigated to using the menu marked “Def File Selection”. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.
- **Navigate to def file.** Select from the Def File Selection menu

3.3 File Locations

This demo kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z11DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z11 register definition files and configuration files:
    - .\cfg_demo_gui\DS33Z11_cfg_demo_gui\DS33Z11.def
    - .\DS33Z11_cfg_demo_gui\SU_LI_PORT1.def
    - .\DS33Z11_cfg_demo_gui\basic_config.mfg

- DS2155 register definition files and configuration files:
    - .\DS33Z11_cfg_demo_gui\te1_ds2155\DS2155.def
    - .\DS33Z11_cfg_demo_gui\te1_ds2155\e1_gapclk_crc4_hdb3_nocas.ini

- DS3170 register definition files and configuration files:
    - .\DS33Z11_cfg_demo_gui\te3_ds3170\ _DS3170_Global.def
    - .\DS33Z11_cfg_demo_gui\te3_ds3170\ DS3170_Port_LIU.def
    - ….. 6 other low level def files ….
    - .\DS33Z11_cfg_demo_gui\te3_ds3170\70_t3_sct_needscoaxlb.mfg

4. Basic DS33Z11 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the DS33Z11. Any one of these initializations can be used with the following Quick Setup examples:

1. Device driver based. If pins J04.1+J04.2 are jumpered, the on-board device driver provides a basic configuration for the DS33Z11. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Sections 4.1 and 4.2 describe specific device driver based configurations. To load the GUI interface for the device drivers go to the ChipView register mode Tools menu and select Tools→Plugins→DS33XW Device Driver Demo.
2. Register-Based Configuration. Launch ChipView.exe and select *Register View.* Sections 4.3 and 4.4 describe specific configurations.
3. Hardware Mode. Set switches as described in the section for powering up the demo kit, then change the following: HWMODE←3.3V, A0←3.3VV, A1←3.3V, A2←0V. This sets the part for LSB first, scrambling off, HDLC encapsulated. At this point traffic will pass from the Ethernet port to the serial port. In this mode broadcast frames are not passed (i.e., ping).
4. EEPROM mode is available with the DK, but is beyond the scope of this manual.

4.1 Quick Setup #1 (Device Driver + T1 or E1)

- Install jumpers to place the serial interface in T1E1 mode as shown in Figure 1.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as described in the previous section. (Ensure jumpers for J04.1+J01.2 are installed to enable the device driver).
- Remove jumper between J04.9 and J04.10:
- Install jumper between J04.7 and J04.8 for E1 mode. Remove jumper between J04.7 and J04.8 for T1 mode.
- Place a loopback connector at the DS2155 network side; RLOS LED DS13 should go out.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the ACT LED to blink.
- To interact with the device driver select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
  - A new form called ‘Zchip Configuration’ pops up.
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the ‘Zchip Configuration’ form). Select the file named ‘basic_Config.eset’

4.2 Quick Setup #2 (Device Driver + T3 or E3)

- Install jumpers to place the serial interface in T3E3 mode as shown in Figure 1.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as described in the previous section. (Ensure jumpers for J04.1+J01.2 are installed to enable the device driver).
- Install jumper between J04.9 and J04.10:
- Install jumper between J04.7 and J04.8 for E3 mode. Remove jumper between J04.7 and J04.8 for T3 mode.
- Place jumpers to loopback the DS3170 network side; RLOS LED DS12 should go out.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the ACT LED to blink.
- To interact with the device driver select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
  - A new form called ‘Zchip Configuration’ pops up.
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the ‘Zchip Configuration’ form). Select the file named ‘basic_Config.eset’

4.3 Quick Setup #3 (DS2155 T1E1)

- Install jumpers to place the serial interface in T1E1 mode as shown in Figure 1.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as previously described.
- Launch ChipView.exe (or use existing session if its already open) and select *Register View.* When prompted for a definition file, pick the file named **DS33Z11.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **basic_config.mfg**.
- Load the definition file for the DS2155 by going to the file menu and selecting File→Definition Config File and select the definition file named **DS2155.def**. After the definition file loads, go to the File menu and select File→Reg Ini File→Load Ini File. When prompted, pick the file named **e1_gapclk_crc4_hdb3_nocas.ini**.
- Place a loopback connector at the DS2155 network side; RLOS LED DS35 should go out.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the ACT LED to blink.

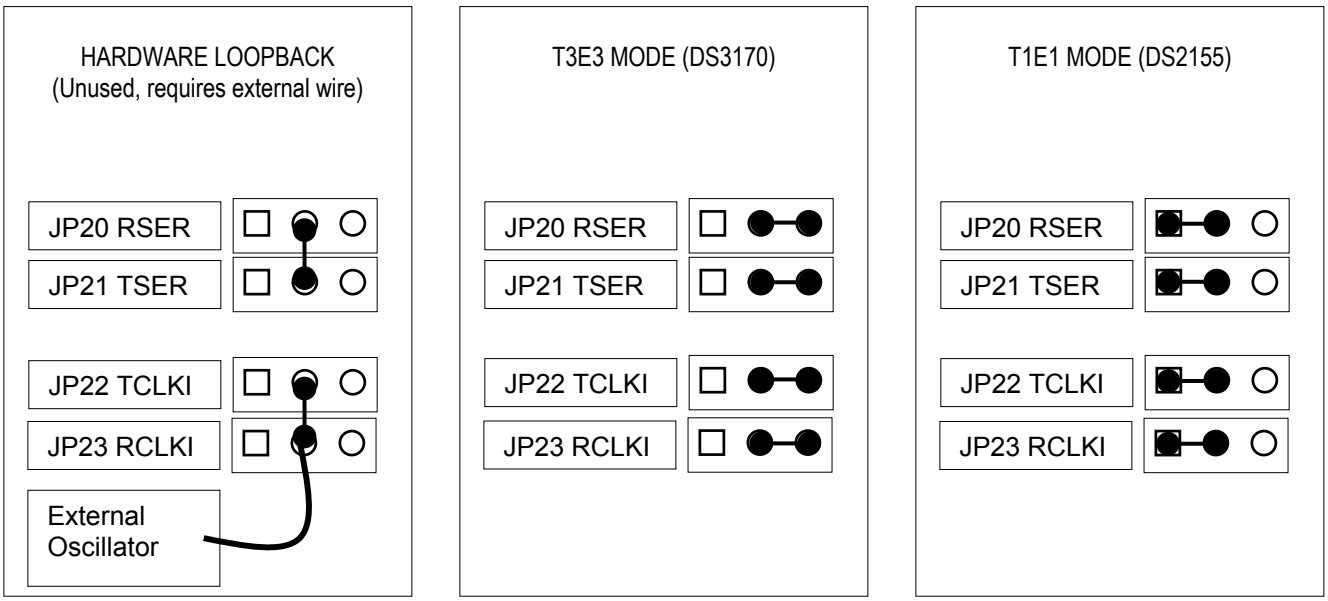
4.4 Quick Setup #4 (DS3170 T3E3)

- Install jumpers to place the serial interface in T3E3 mode as shown in Figure 1.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as previously described.
- Launch ChipView.exe (or use existing session if its already open) and select *Register View.* When prompted for a definition file, pick the file named **DS33Z11.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **basic_config.mfg**.
- Load the definition file for the DS3170 by going to the file menu and selecting File→Definition Config File and select the definition file named **ds3170_global.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **70_t3_sct_needscoaxlb.mfg**.
- Place a loopback connector at the DS3170 network side.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the ACT LED to blink.

5. Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is *not* recommended. The ping command goes through the computer's TCPIP stack, and sometimes will not be sent out the PC's network connector (i.e., if the PCs' ARP cache is out of date). Additionally ping requires two PCs, as a PC with only one adapter can not ping itself (a local ping gets sent to 'local host' instead of out the connector). With that said, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be easily accomplished using CommView. A time-limited demo is available at the website www.tamos.com/products/commview.
- Wireshark is an excellent (and free) packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters the PC will have a different IP address for each adapter. Test equipment will allow selection of either adapter. Operating system based network traffic will be sent out the default adapter, usually this is the adapter that has recently had connection to a live network.

Figure 1. Serial Jumper Configuration



6. LEDs Configuration Switches and Jumpers

The DS33Z11DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 1 provides a description of these components, given in order of appearance on the PCB. Component listing is given from left to right, top to bottom, when the board is held with the Ethernet port at the top.

Table 1. Main Board PCB Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J01	System Power	Installed	Installed	Power jack +5.0V to center post
J02	Ethernet Connection	Installed	Installed	Ethernet connection with MDIX, connect with ether a patch or crossover cable
JP01 JP02 JP03	DP83848 AN0 AN1 AN_EN	Not installed *	Not installed*	Configuration pins for DP83848 PHY. These pins have internal pullups. Leaving un-Jumpered or setting to VCC enables auto-negotiation and advertise as 100/10 full/half duplex capable.
DS02+DS01 DS04+DS03 DS06+DS05	Link (on for link) Speed (on for 100) Activity (blink for act)	On On Blink	On On Blink	Status LEDs for DP83848 PHY. Each status function has 2 LEDs to accommodate the pin configuration methods used by the PHY
JP12	DP83848 MDIX	VCC	VCC	Set to VCC to enable MDIX (automatic crossing of RX/TX pair)
JP14	DP83848 RMII	GND	GND	Set to GND to enable MII mode, VCC to enable RMII mode. Note that the DS33Z11 RMII pin needs to be Jumpered to match this pin.
JP11	DS33Z11 mode pin; DTE/DCE selection	Low	Low	Low for DTE
JP10	DS33Z11 mode pin RMII/MII selection	Low	Low	High for RMII, low for MII

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
JP09	DS33Z11 mode pin CKPHA selection	Low	Low	SPI EEPROM hardware mode configuration switch
JP08	DS33Z11 mode pin MODEC0 selection	High	Low	Software mode selected
JP07	DS33Z11 mode pin MODEC1selection	Low	Low	Software mode selected
JP06	DS33Z11 mode pin HWMODE selection	Low	Low	Hardware/software mode (software mode selected)
JP04	DS33Z11 mode pin SCANMO selection	Low	Low	Set low for normal operation
JP05	DS33Z11 mode pin SCANEN selection	Low	Low	Set low for normal operation
J03	USB	User decision	User decision	System USB connector. Used with ChipView host PC software (if RS232 is not used)
J10	RS232 Serial	User decision	User decision	System RS232 connector. Used with ChipView host PC software (if USB is not used). The RS232 connector may also be used with any terminal emulator, settings are 57.6K, 8N1, no flow control.
DS07	Status LED	On	On	Displays kit status. This LED should remain lit
DS08	Status LED	-	-	Miscellaneous LED.
J04.1 + J04.2	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z11 and the transceiver during power-up.
J04.3 + J04.4	Enable callbacks	User decision	—	When installed the driver will respond to interrupts.
J04.3 + J04.4	Looptime / Sourcetime	User decision	—	When installed the driver will configure the serial link for Looptime (TCLK driven by RCLK). When not installed TCLK is driven by scaled MCLK. Driver must be enabled to make use of this setting.
J04.7 + J04.8 J04.9 + J04.10	T1E1, T3E3 selection	Not installed	—	When installed the driver will select a transceiver and mode of operation as shown below. 00 = DS2155 in T1 Mode 01 = DS3170 in T3 Mode 10 = DS2155 in E1 Mode 11 = DS3170 in E3 Mode Driver must be enabled to make use of these settings.
JP18 JP17 JP16	Addr2 Addr1 Addr0	Installed Pins 2+3	See DS33Z11 datasheet	Address pin/EEPROM config switch. Install on pins 2+3 to connect DS33Z11 address pins A2,A1,A0 to the processor. Leave disconnected to allow pullup to pull high. Connect pins 1+2 to pull low.
J07	JTAG	—	—	JTAG testpoints for DS33Z11
J06, J05	Ethernet Testpoints	—	—	Testpoints for Ethernet interface
YB02 (Bottom side)	Unused refclk OSC	—	—	Unused oscillator. Could be used to drive DS33Z11 refclk and PHY MCLK. Instead this oscillator is not used, and the clocks are provided by DS33Z11 RefClkO.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
JP24	RefClk / Phy Clock selection	—	—	DS33Z11 RefClk output. Jumper pins 1+2 to drive with YB02. Jumper pins 2+3 to drive with DS33Z11 RefClk output.
YB03 (Bottom side)	System Clock	—	—	System Clock for DS33Z11. Must be set for 100Mhz If RefClkO is used to drive RefClkI and PhyClk.
Y01 (Not populated)	spi_cs, spi_ck, spi_miso, spi_mosi	—	—	SPI signals (for EEPROM memory)
JP13	DS33Z11 mode pin AFCS selection	HW mode only	High	Set high to enable auto flow control.
JP15	DS33Z11 mode pin FULLDS selection	HW mode only	High	Set high to enable full duplex.
JP19	DS33Z11 mode pin H10S selection	HW mode only	High	Set high to confg for 100Mb
U04	Processor testpoints	--	--	Testpoint grid surrounding processor, all processor pins are brought out.
J09 J08	Address Databus	—	—	Address databus for DS33Z11, DS2155, DS3170. Unused chipselect CS_X4 are provided to allow the DK to control additional, external devices.
J08.12+J08.14	FPGA Tristate Jumper	—	—	Setting the 'tristate' jumper will tristate the FPGA. This provides the user with a method for controlling the DK with an external processor.
TP02	RefClkIn Testpoint	—	—	DS33Z11 RefClk input. Also see JP24.
SW01	System Reset	—	—	Drives UB11 reset controller
DS11	LED	—	—	Power OK LED
J13	Debug	—	—	Connector for OnCe software debug
J12	JTAG	—	—	JTAG connector for Lattice FPGA
TP05 TP06	TDEN RDEN	—	—	DS33Z11 TDEN RDEN testpoints. Unused.
JP20 JP21 JP22 JP23	TSER RSER TCLKI RCLKI	Jumpered, See Figure 1	Jumpered, See Figure 1	Jumper selection for serial interface. Possible modes are: T1E1, T3E3, Loopback (or wired to external system). Note that loopback requires an external oscillator to be wired in.
JP25	Testpoints T3E3_OSC	—	—	Testpoints for T3E3 Oscillator. Can be used as TCLK/RCLK when in hardware loopback
YB04	OSC	—	—	Oscillator for DS2155 MCLK
J14 J16	2-pin BNC Jumper	—	—	Jumper for connection to T1E1 BNC
J15	RJ45	—	—	T1E1 RJ45 connector
DS13	LED	—	—	DS2155 RLOS LED
DS12	LED	—	—	DS3170 GPIO LED
J18 J17	TX RX	—	—	Jumper for connection to T3E3 BNC

7. Address Map

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to 0x81000000.

Table 2. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z11	DS33Z11. Uses CS_X1.
0X2000 to 0X2FFF	DS2155	T1E1 transceiver. Uses CS_X2
0X3000 to 0X3FFF	DS3170	T3E3 transceiver. Uses CS_X3.
0X4000 to 0X4FFF	Unused	Unused chipselect for controlling external device. Uses CS_X4.

Registers in the DS33Z11, DS2155, and DS3170 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

8. DS33Z11 Information

For more information about the DS33Z11, consult the DS33Z11 data sheet available on our website at www.maxim-ic.com/DS33Z11.

8.1 DS33Z11DK Information

For more information about the DS33Z11DK, including software downloads, consult the DS33Z11DK data sheet available on the our website at www.maxim-ic.com/DS33Z11DK.

8.2 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

9. Component List

Table 3 shows the component list for the DS33Z11DK.

Table 3. Component List

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C01, C02, C03, C04, C05, C06, C07, CB22, CB28, CB73 , C14, C16, C20, CB44, CB56	15	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
See next row (begins with C08)	34	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C08, C17, C22, C27, C29, C36, C37, C40, C41, C42, CB05, CB11, CB17, CB18, CB19, CB27, CB35, CB40, CB46, CB47, CB54, CB57, CB59, CB65, CB69, CB78, CB80, CB82, CB84, CB90, CB91, CB94, CB97, CB99				
	31	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C09, C18, C24, C38, C39, C45, CB08, CB13, CB29, CB32, CB33, CB34, CB37, CB39, CB45, CB50, CB55, CB58, CB60, CB63, CB67, CB70, CB71, CB74, CB76, CB86, CB87, CB88, CB93, CB95, CB96				
C10, C11	2	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C12, C13 , C44	3	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
See next row (begins with C15)	51	0603 CERAM 4.7uF 6.3V MULTILAYER	UNK	ECJ-1VB0J475M
C15, C21, C23, C25, C26, C28, C30, C31, C32, C33, C34, C35, C43, C46, C47, CB09, CB10, CB15, CB20, CB21, CB24, CB25, CB26, CB30, CB31, CB36, CB38, CB41, CB42, CB43, CB48, CB49, CB51, CB52, CB53, CB61, CB62, CB64, CB66, CB68, CB72, CB75, CB77, CB79, CB81, CB83, CB85, CB89, CB92, CB98, CB100				
C19, CB04, CB06, CB07, CB14, CB16, CB23	7	0603 CERAM 0.1uF 16V 10%	Phycomp	06032R104K7B20D
CB01, CB02, CB03, CB12	4	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
DB01	1	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS02, DS07 , DS11	4	L_LED, GREEN, SMD	Panasonic	LN1351C
DS03, DS04	2	LED, AMBER, SMD	Panasonic	LN1451C
DS05, DS06, DS13 , DS08, DS09, DS10, DS12	7	LED, RED, SMD	Panasonic	LN1251C
GND_TP01, GND_TP02, GND_TP03, GND_TP04, GND_TP05, GND_TPB01	6	STANDARD GROUND CLIP	KEYSTONE	4954
H01, H02, H03, H04, H05, H06	6	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	4-40KIT4
J01	1	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	CUI, INC	PJ-002AH
J02	1	CONNECTOR, FASTJACK SINGLE, 8 PIN FOR NATIONAL PHY	Halo Electronics	HFJ11-2450E
J03	1	TYPE B SINGLE RT ANGLE, BLACK	MOL	NA
J04	1	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	NA
J05, J06	2	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE	DNP	DNP

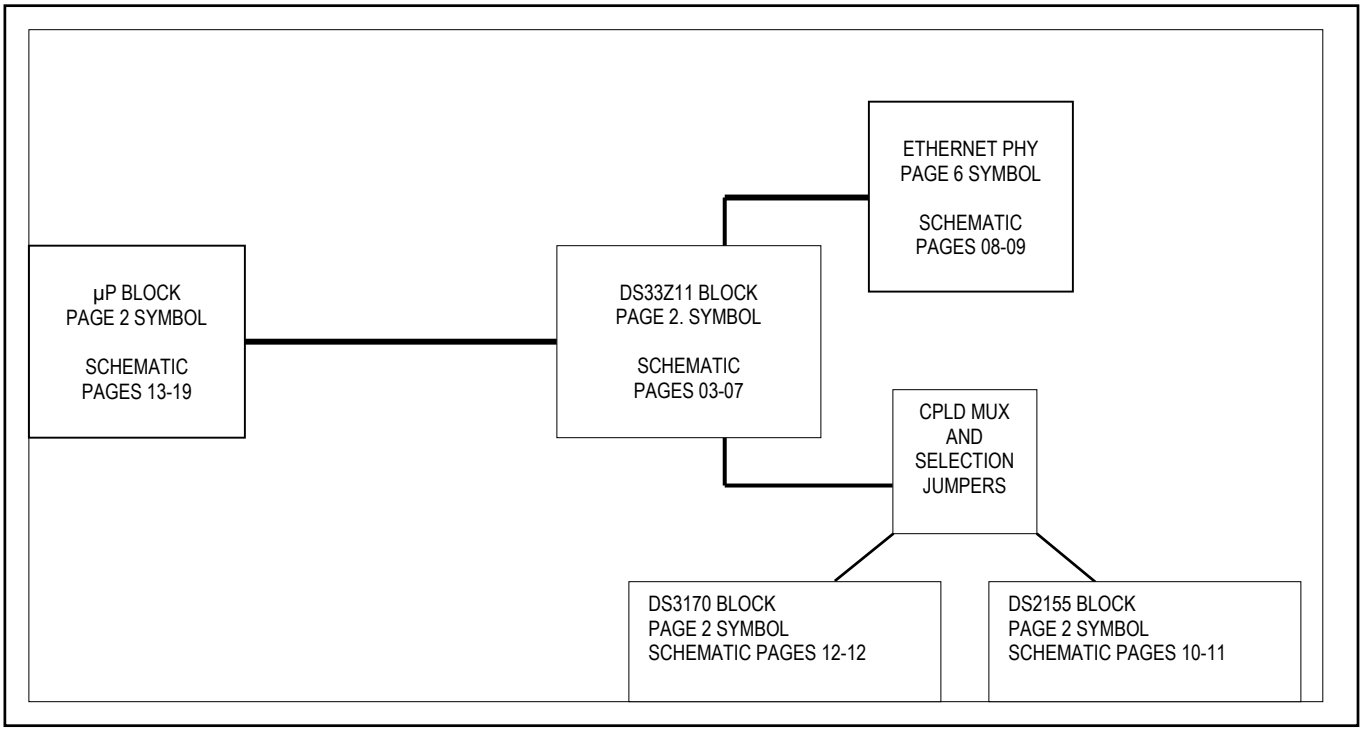
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
J07, J12	2	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J08, J09	2	NON POPULATED HEADER, 14 PIN, DUAL ROW, VERT	Samtec	NOPOP-HDR-TSW-107-14-T-D
J10	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J11	1	100 MIL 2 POS JUMPER	NA	NA
J13	1	100 MIL 2*7 POS JUMPER	NA	NA
J14, J16, J17, J18	4	L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	TSW-102-07-T-S
J15	1	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
See next row (begins with JP01)	23	100 MIL 3 POS JUMPER	NA	NA
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24				
R01, R1, R2, R3, R4, R5, R6, R7, R8, R9, R05, R15, R16, R17, R18, RB06, RB16	17	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
R02, RB25, RB26, RB29, RB43 , RB24	6	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
See next row (begins with R03)	19	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R03, R04, R06, R07, RB32, RB36, RB37, RB38, RB39, RB40 , R13, RB19, RB21, RB23, RB41, RB42, RB48, RB53, RB54				
R09	1	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R10, R11, R12, R14	4	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
RB01, RB02, RB03, RB04, RB05, RB22, RB34	7	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
RB07	1	RES 0603 4.87K Ohm 1/16W 1%	Panasonic	ERJ-3EKF4871V
RB18, RB20 , RB28, RB30, RB35, RB51	6	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB33	1	RES 0805 10K Ohm 1/10W 1%	Panasonic	ERJ-6ENF1002V
RB44, RB46	2	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB49, RB50	2	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
RB52	1	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RP01	1	4 PACK RESISTOR 50 OHM 2 PCT	KOA	CN1J4TTD500G OR CN1J4TTD49R9F
RP02, RPB01, RPB03, RPB04, RPB05	5	4 PACK RESISTOR 2.2K OHM 5% QUAD 0402	PANASONIC	EXB-N8V222JX
RP03, RP04, RP05, RPB06	4	4 PACK RESISTOR 30 OHM 5% QUAD 0402	PANASONIC	EXB-N8V300JX
See next row (begins with RP06)	17	4 PACK RESISTOR 10K OHM 5% QUAD 0402	PANASONIC	EXB-N8V103JX
RP06, RP07, RP08, RPB08, RPB09, RPB10, RPB11, RPB12, RPB13, RPB14, RPB16, RPB17, RPB18, RPB19, RPB20, RPB21, RPB22				
RPB02, RPB07, RPB15	3	4 PACK RESISTOR 330 OHM 5% QUAD 0402	PANASONIC	EXB-N8V331JX
SW01	1	L_SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
T01	1	XFMR 16P SMT	Pulse	TX1099

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
T02	1	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01, TP02, TP03, TP04, TP05, TP06, TPB01, TPB02, TPB03, TPB04	10	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U01	1	IC, DP83848C PHYTER 10/100 ETHERNET TRANSCEIVER, 48 PIN TQFP	National Semiconductor	DP83848C
U02	1	USB UART (USB - 8 bit FIFO), 32 PIN LQFP	FTD	FT245BM
U03	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Maxim	DS33Z11
U04	1	MMC2107 PROCESSOR	Motorola	MMC2107
U05	1	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	LAT	LFEC3E-3T144C
U06, UB13	2	CYPRESS SRAM, LAB STOCK	NA	NA
U07	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Maxim	DS3170
U08	1	T1/E1/J1 XCVR 100P QFP 0-70C	Maxim	DS2156L
UB01, UB02, UB03, UB04	4	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB05	1	8-Pin uMax SOIC 1.8V or Adj	Maxim	MAX1792EUA18
UB06	1	SPI SERIAL EEPROM 2M 8 PIN SOIC 2.7V to 3.6V	Atmel	AT25F2048N-10SU-2.7
UB07, UB12 , UB14	3	HIGH SPEED BUFFER	FAIRCHILD	NC7SZ86
UB08	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	NA
UB09	1	IC, LDO REGULATOR WITH RESET,1.20V OUTPUT 300 MA, 6 PIN SOT23	Maxim	MAX1963EZT120-T
UB10	1	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7
UB11	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	Maxim	MAX811TEUS-T
XB01	1	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01	1	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V SOCKET ONLY	Atmel	AT25160A-10PI-2.7
YB01	1	XTAL, LOW PROFILE, 6.00 MHZ	Pletronics	LP49-26-6.00M
YB02	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V socket	SaRonix	NA
YB03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
YB04	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
YB05	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736

10. Schematics

The DS33Z11DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of three hierarchal blocks: the processor block, the DS33Z11 block, and an Ethernet block inside the DS33Z11 block, which is a nested hierarchy block. The serial card consists of two hierarchy blocks, one for each of the DS2155, and DS3170. These blocks are connected by jumpers to the DS33Z11.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.



11. Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
031405	Initial DS33Z11DK data sheet release.	—
042205	Updated *Basic DS33Z11 Initialization* section; added step to *Quick Setup #1* section; updated Table 2.	9, 11, 12
110106	Updated schematics.	15–39
080508	Reformatted data sheet to conform to newer template style; updated various sections to include the DS33Z11DK01A0 revision.	All

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

DS33Z11 DESIGN KIT

DS33Z11DK02A0

CONTENTS:

NOTES:

ALL HIERARCHY BLOCK NAMES END IN _DN.
PINS ON HIERARCHY BLOCKS DO NOT HAVE PIN NUMBERS (BUT PINS ON SYMBOLS DO).

SIGNALS INSIDE A HIERARCHY BLOCK ARE LOCAL TO THAT BLOCK
THE SIGNAL _TEMP_ IN BLOCK_A_DN IS DIFFERENT THAN _TEMP_ IN BLOCK_B_DN.

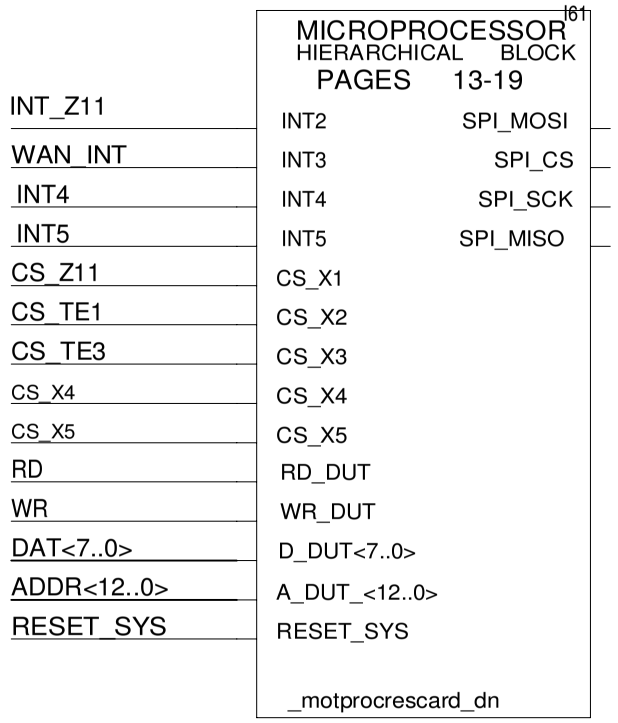
PAGE NUMBERS (BOTTOM RIGHT) ARE LISTED BY BOTH THE PAGE NUMBER IN THE BLOCK,
AND BY THE PAGE NUMBER WITHIN THE ENTIRE DESIGN

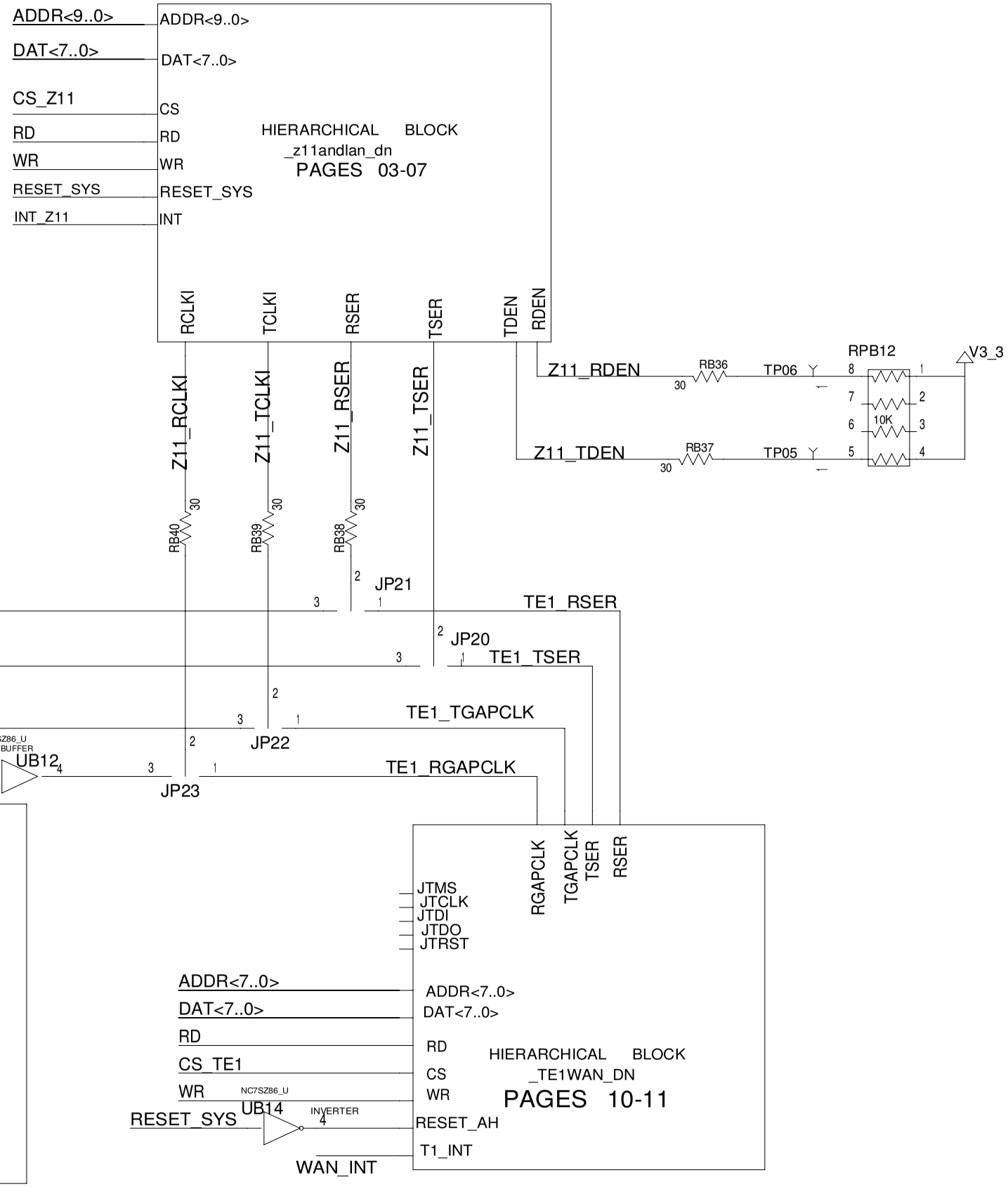
CROSS REFERENCE INDICATORS ARE REFERENCEING A GIVEN NET TO OTHER PAGES IN THE DESIGN
(PAGE NUMBER GIVEN IS ACCORDING TO ENTIRE DESIGN, NOT THE CURRENT BLOCK)

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 1/19(TOTAL)

BLOCK NAME: _ztopdn_.

PRINTED Fri Jun 20 10:05:53 2008

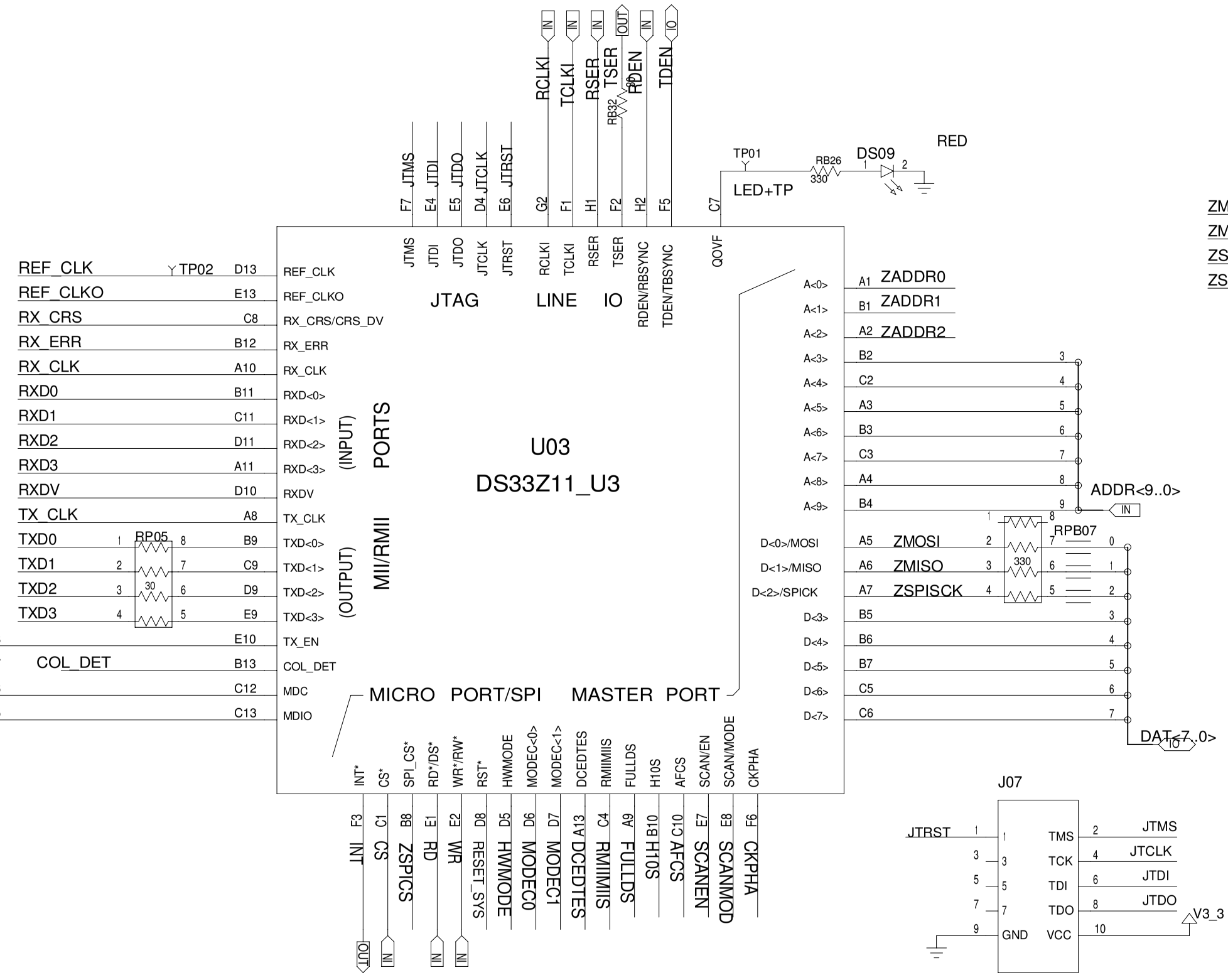




TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 2/19(TOTAL)

BLOCK NAME: _ztopdn_.

DS33Z11

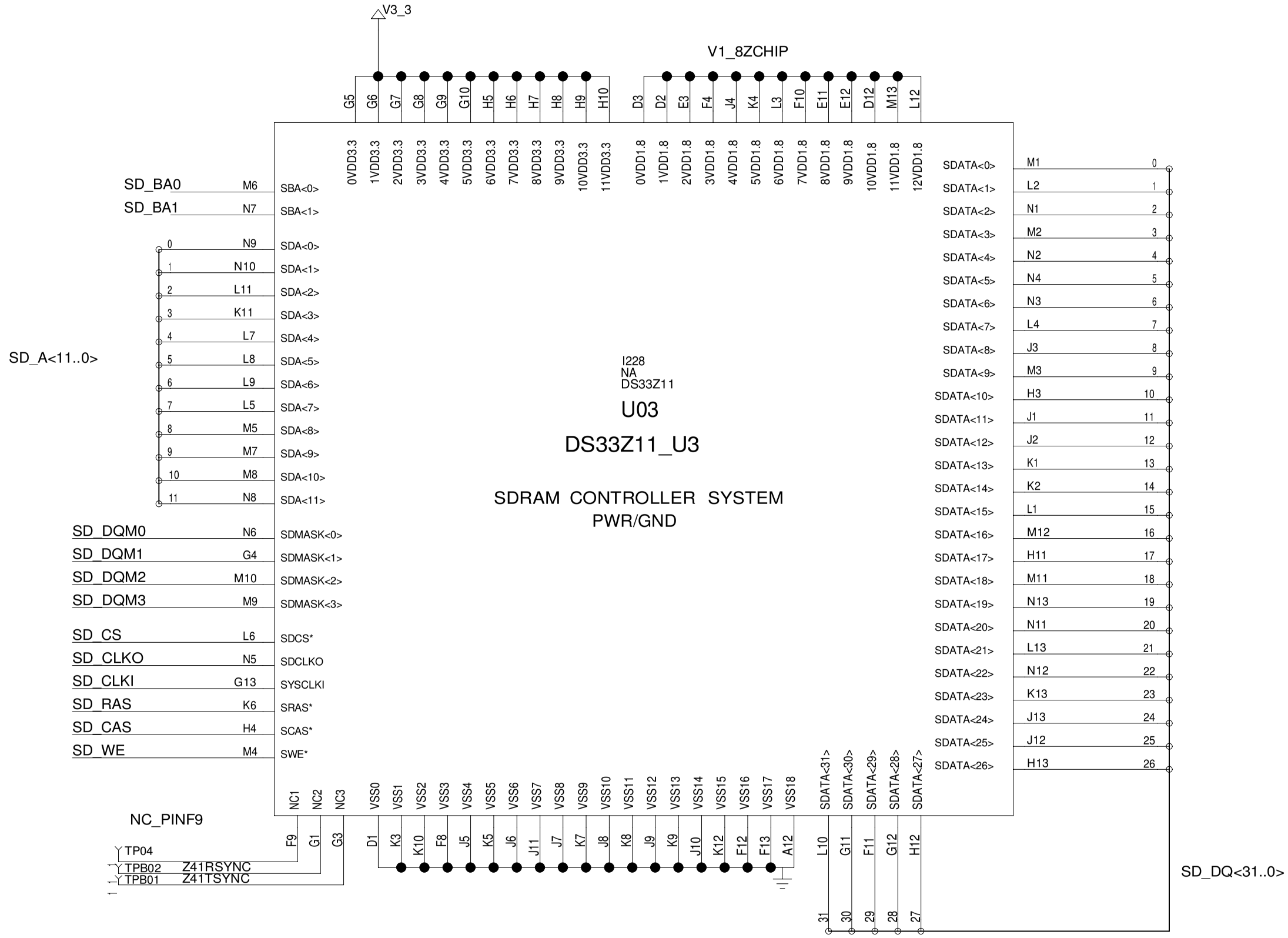


HW MODE PINS ARE OUTPUTS FROM Z MODULE TO PROC
PROC (FPGA) AUTOMATICALY IMPLEMENTS BUS MODE

BEGINNING OF DS33Z11 HIERARCHY BLOCK

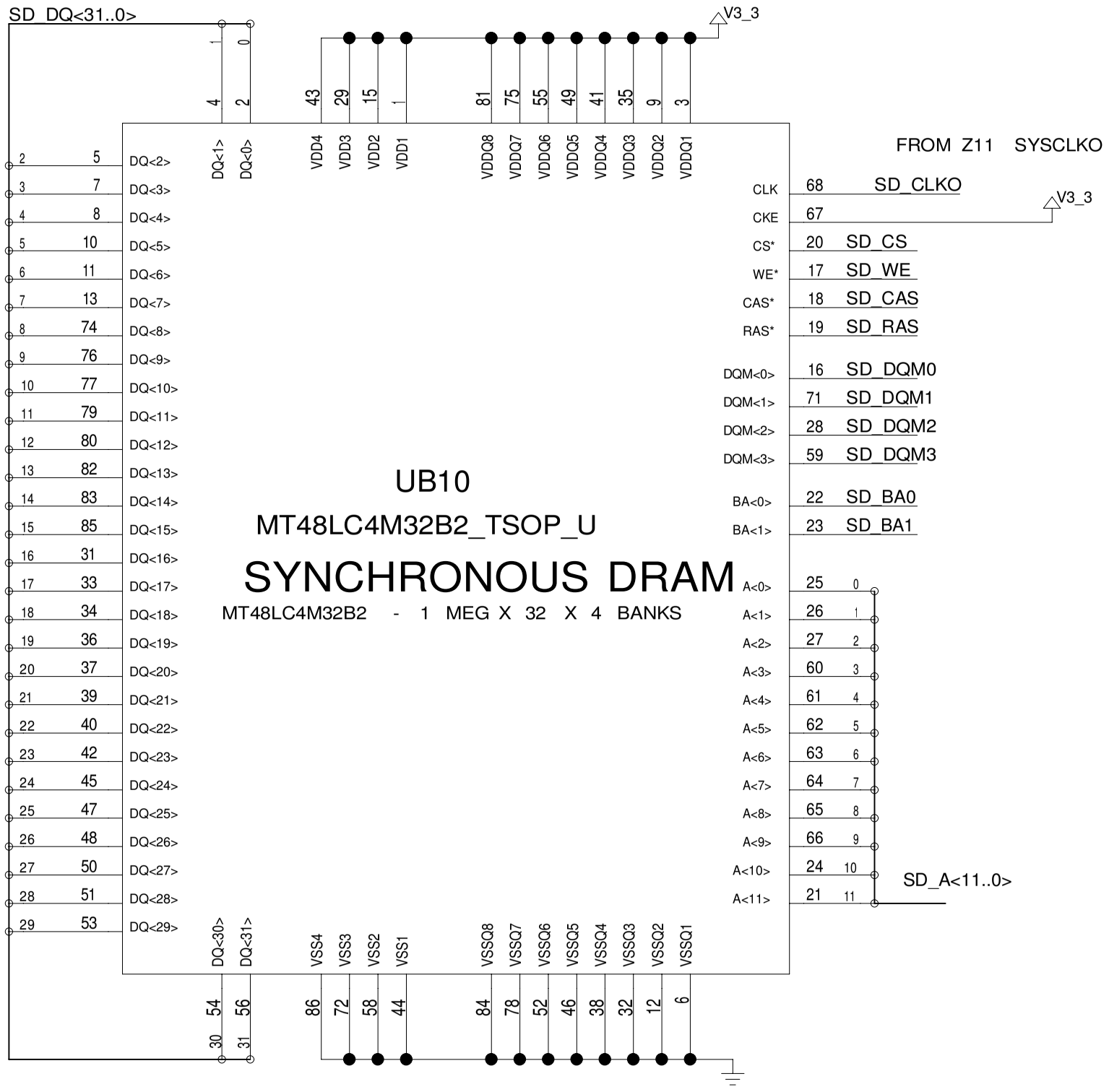
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 3/19(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _ztopdn_\



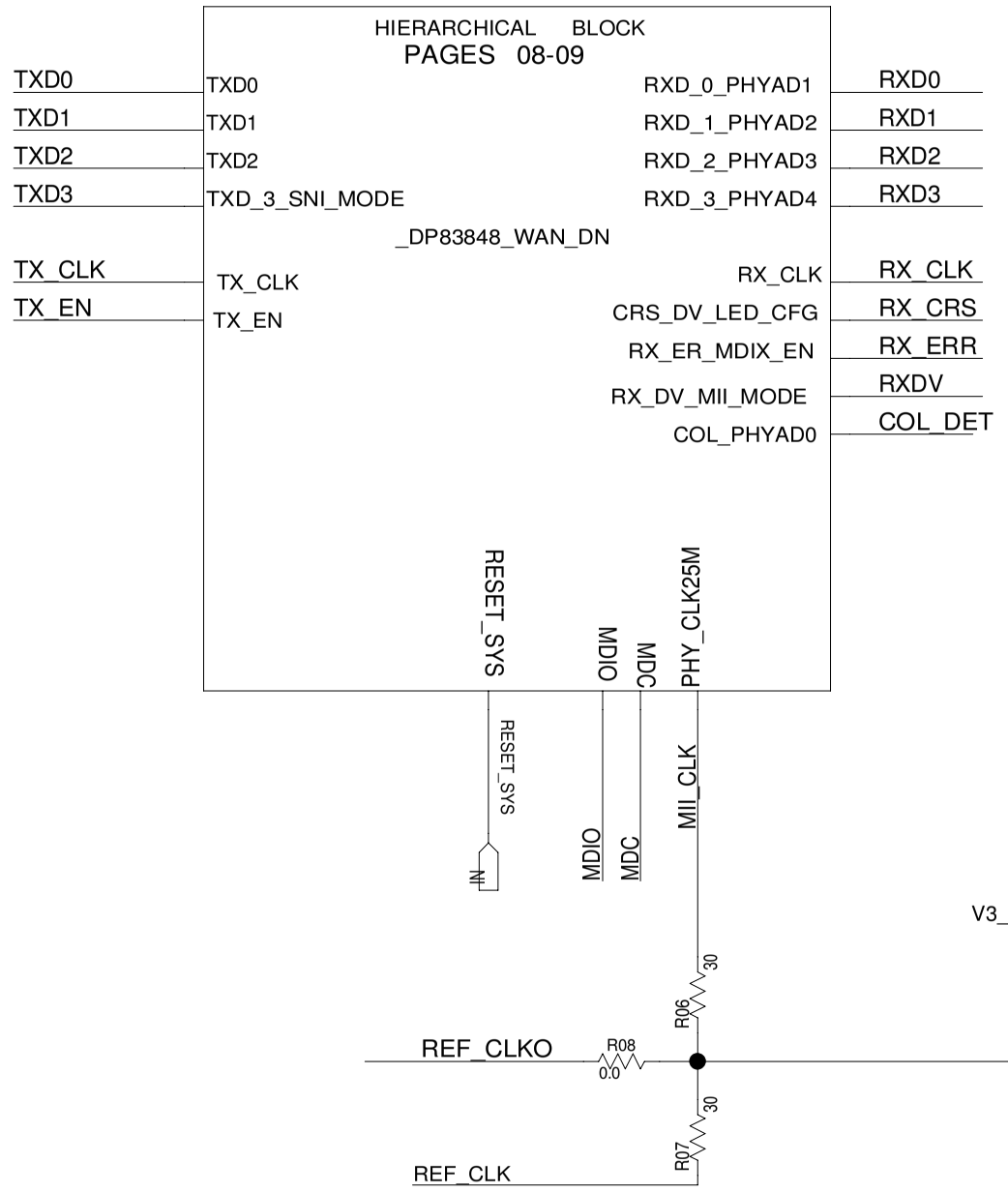
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 4/19(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _ztopdn_\



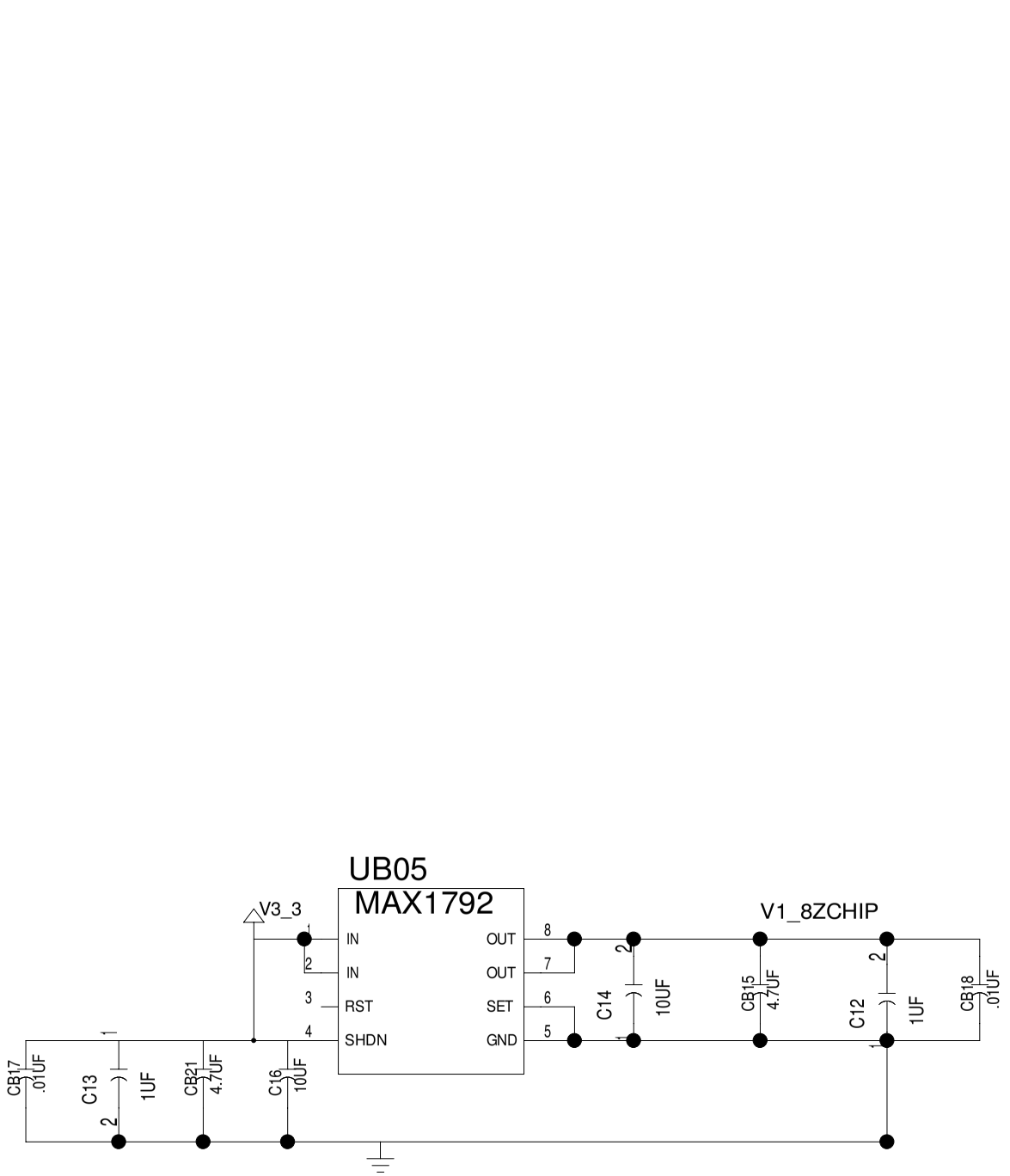
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 5/19(TOTAL)

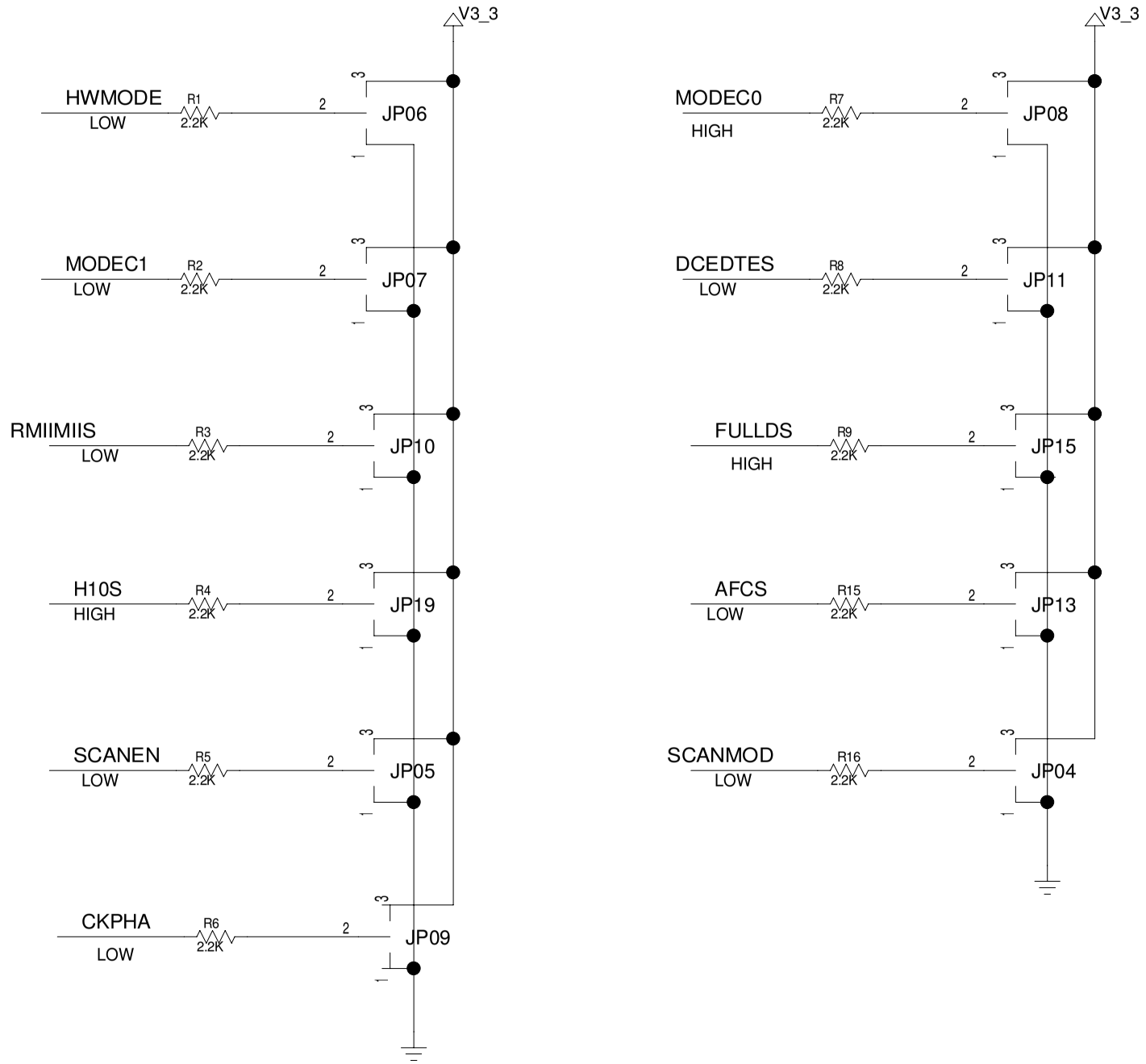
BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _ztopdn_\

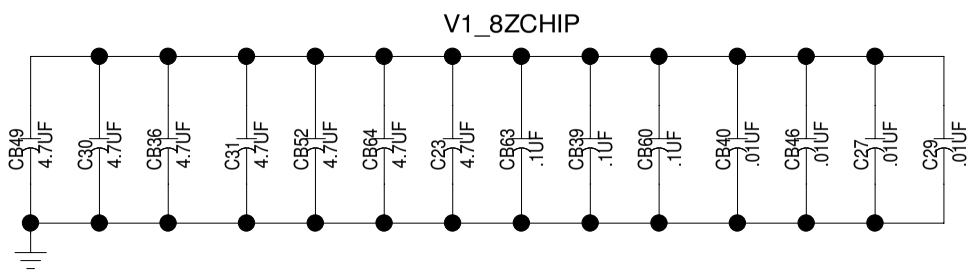


TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 4/5(BLOCK) 6/19(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _ztopdn_\





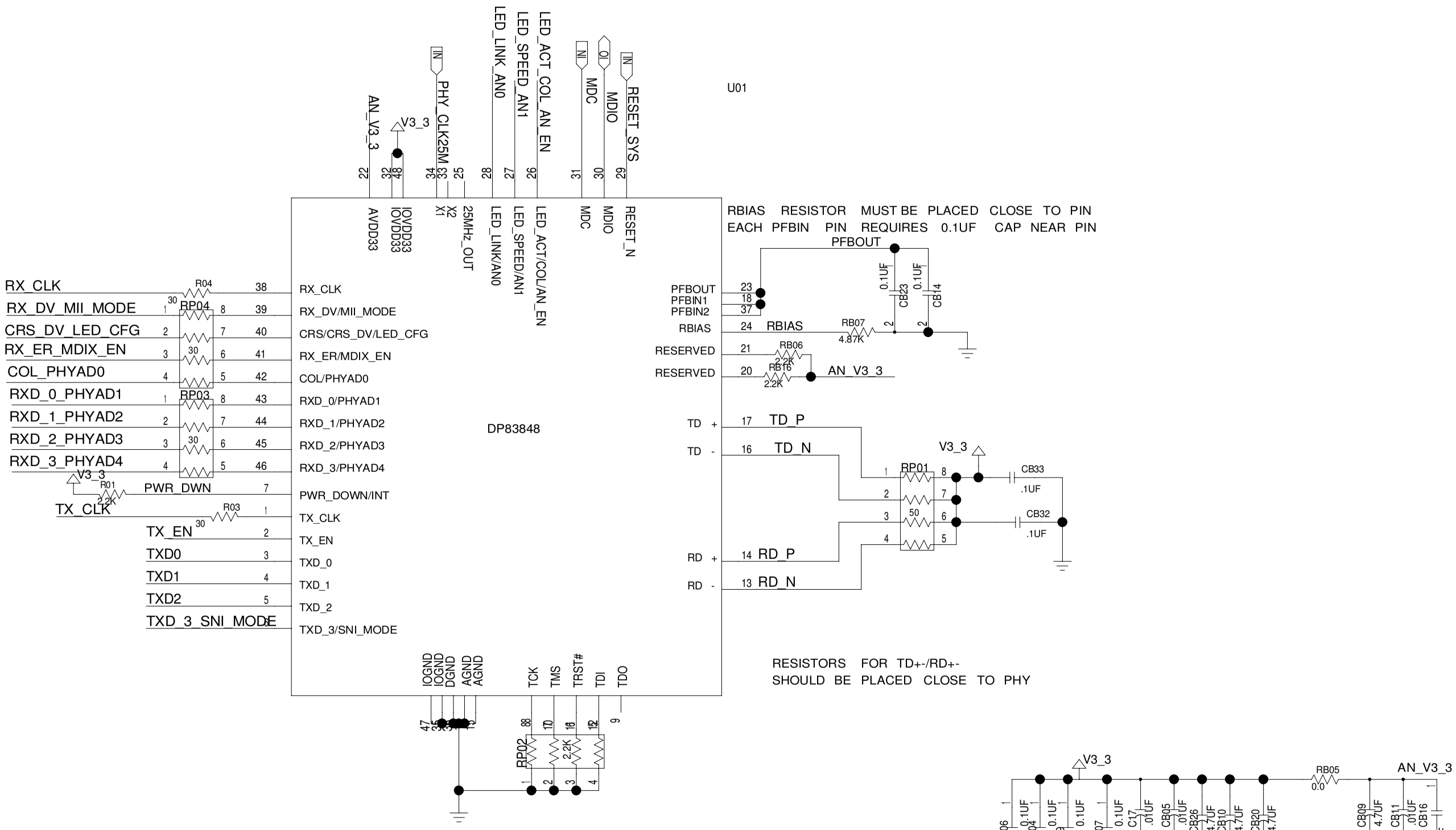


CONFIG SWITCHES FOR Z11
MODE (SHOWN BELOW SIGNAL) RESULTS IN:
MOTOROLA NON-MUX, MII, FULL DUPLEX, 100 MBIT, AUTO-FLOW CONTROL

END OF DS33Z11 HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 7/19(TOTAL)

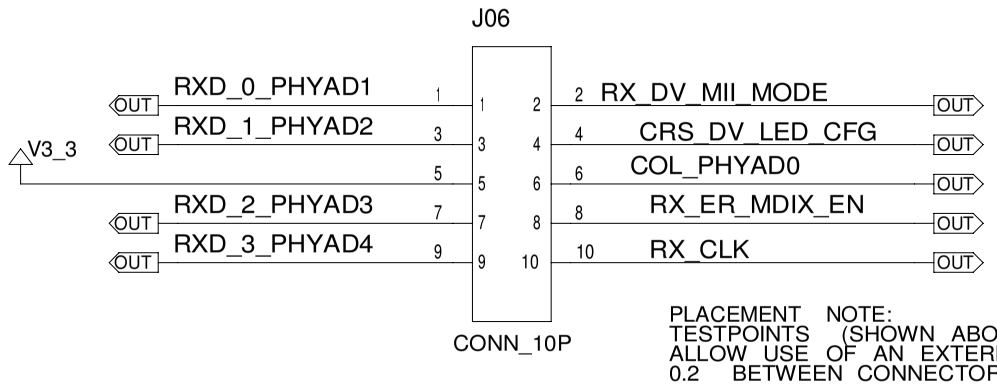
BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _ztopdn_\

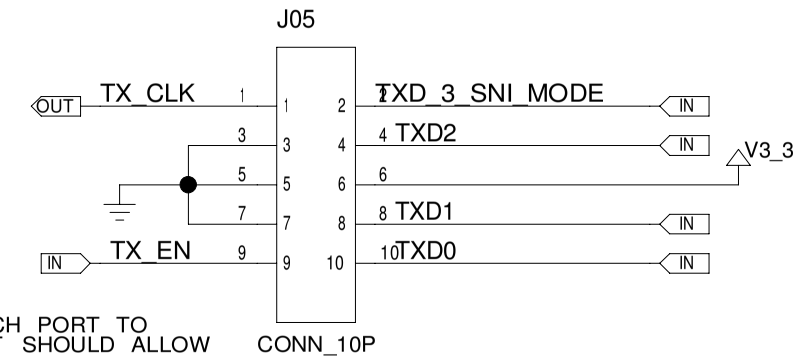


BEGINNING OF PHY HIERARCHY BLOCK

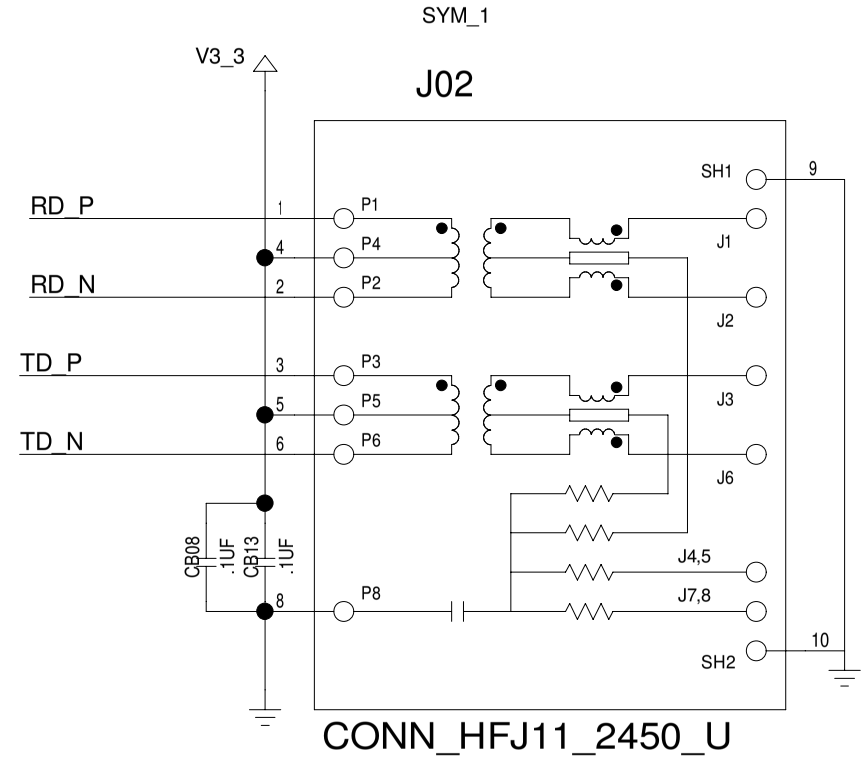
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 8/19(TOTAL)

BLOCK NAME: _dp83848_wan_dn. PARENT BLOCK: _z11andlan_dn\ PRINTED Fri Jun 20 10:04:01 2008

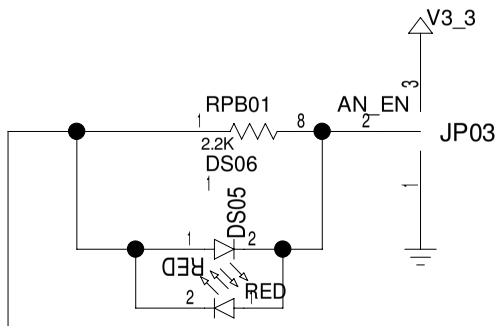


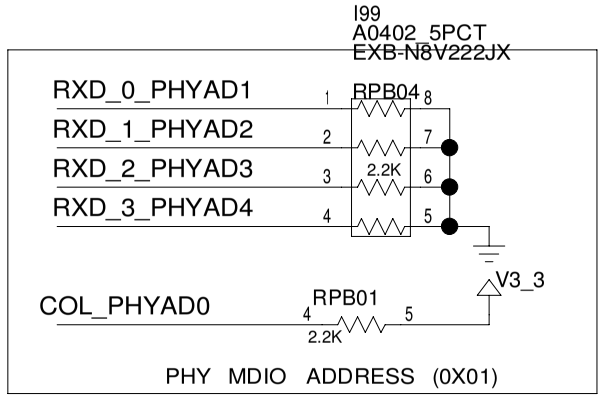


PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO ALLOW USE OF AN EXTERNAL PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW 0.2 BETWEEN CONNECTORS.



CAPS FOR XFRM CENTER TAP SHOULD BE PLACED CLOSE TO XFRM





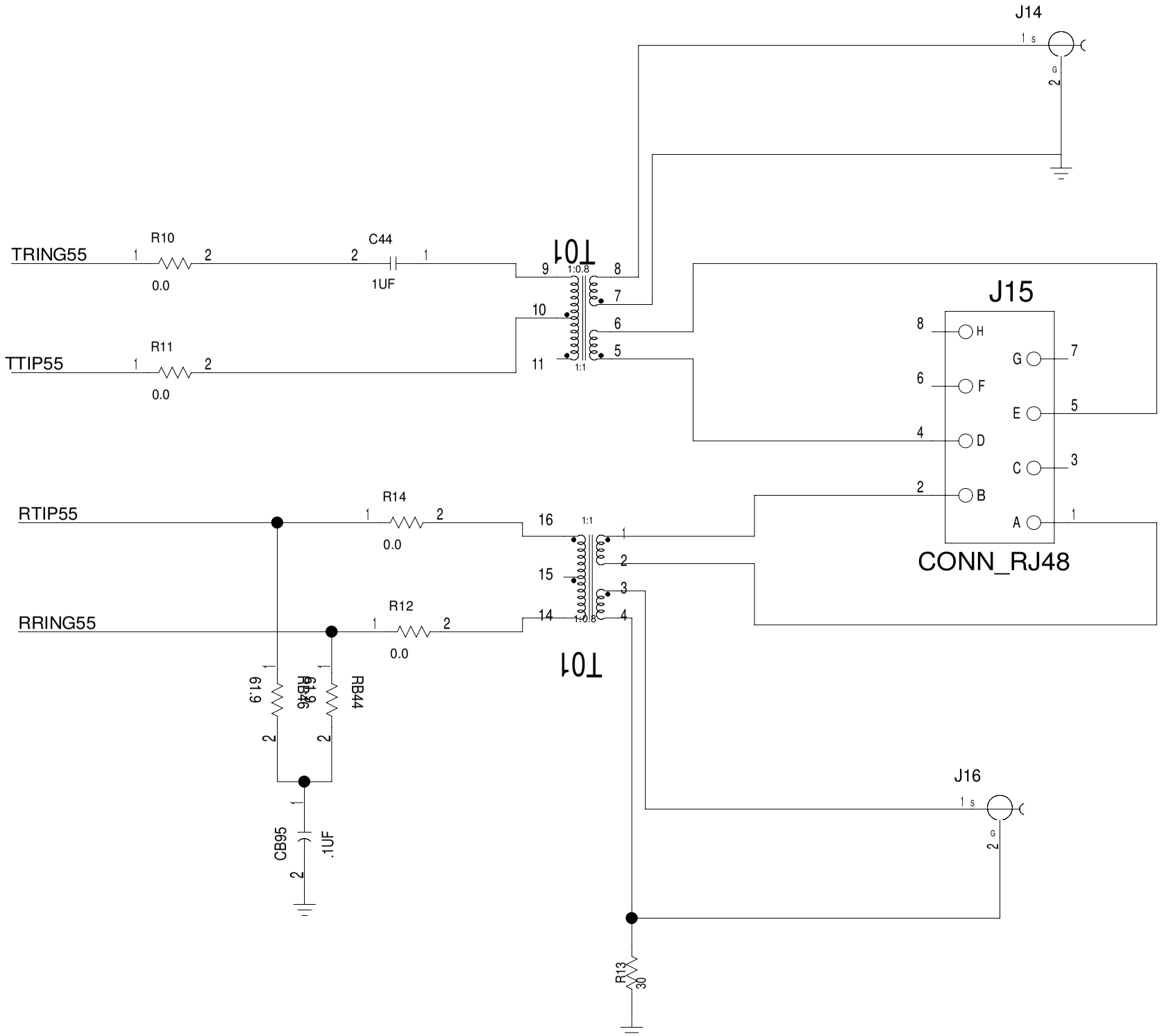
STRAP OPTIONS HERE DO NOT FOLLOW THE DP83484 DATASHEET (SOME PINS HAVE A 2.2K+330 STRAP RESISTOR INSTEAD OF 2.2K)

END OF PHY HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 9/19(TOTAL)

BLOCK NAME: _dp83848_wan_dn. PARENT BLOCK: _z11andlan_dn\

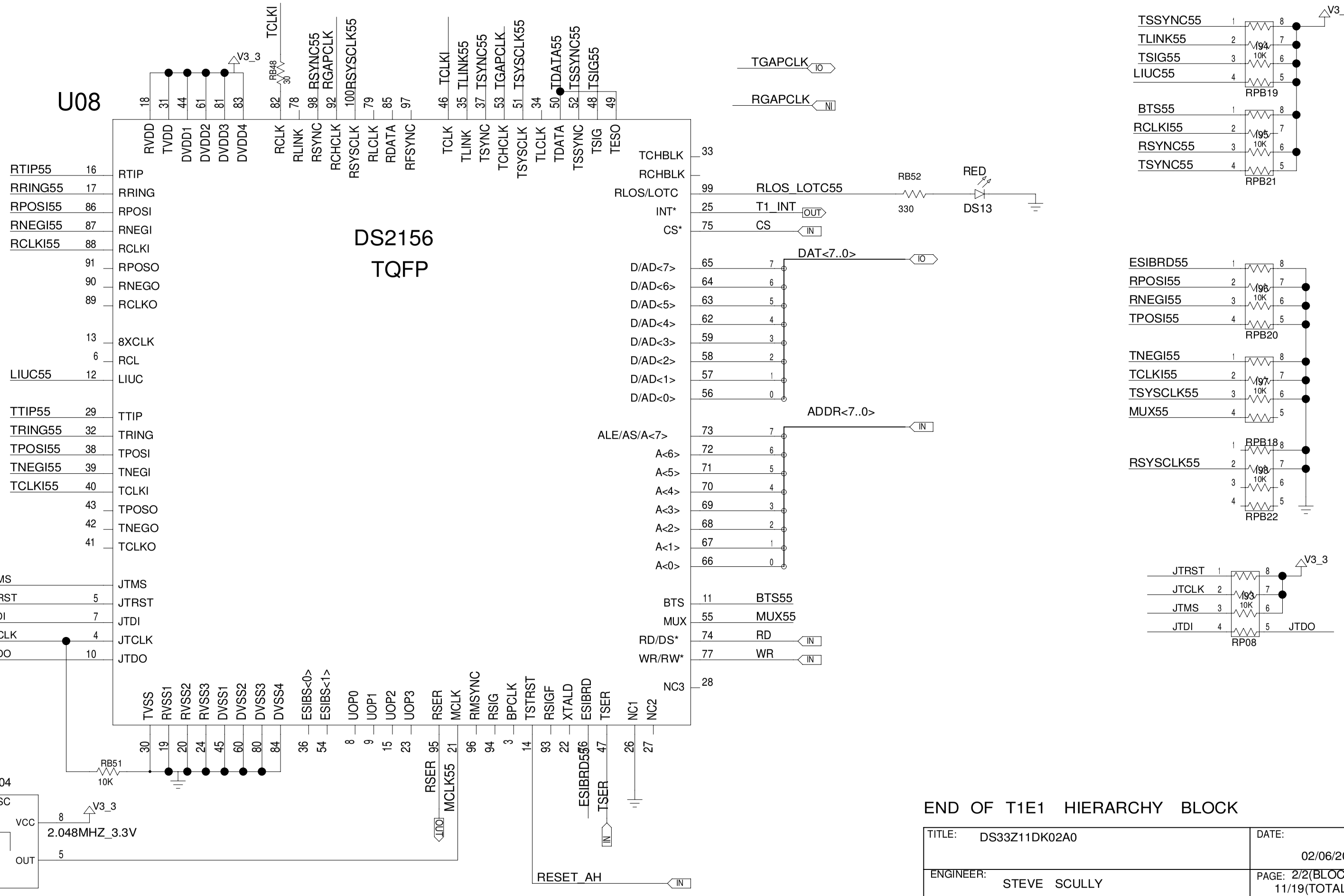
TE1 SINGLE WAN BLOCK



BEGINNING OF T1E1 HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 10/19(TOTAL)

BLOCK NAME: _te1wan_dn. PARENT BLOCK: _ztopdn_\



END OF T1E1 HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 11/19(TOTAL)

BLOCK NAME: _te1wan_dn. PARENT BLOCK: _ztopdn_\

DS33Z11 TE3 WAN BLOCK

(DS3170 SCT, TRANSFORMERS AND CONNECTORS)

44.736MHZ_3.3V

YB05 OSC

V3_3

T3MCLK

ADDR<8..0>

DAT<7..0>

U07

DS3170_BGA_U

HIZ,TEST,ALE

NO TPDENO?

RPB17

RPB16

JTAG TESTPOINTS

RP07

SMT0603_5PCT ERJ-3GEYJ300V

RB41 RB42

TE3_TCLKI

TE3_TXP TE3_TXN TE3_RXP TE3_RXN

T02

J17 J18

75 OHM 2P

TREF1 RREF1

2:1

RB49 RB50 RB54 RB53

RB43

R18 R17

T3_INT MODE WIDTH RESET_SYS

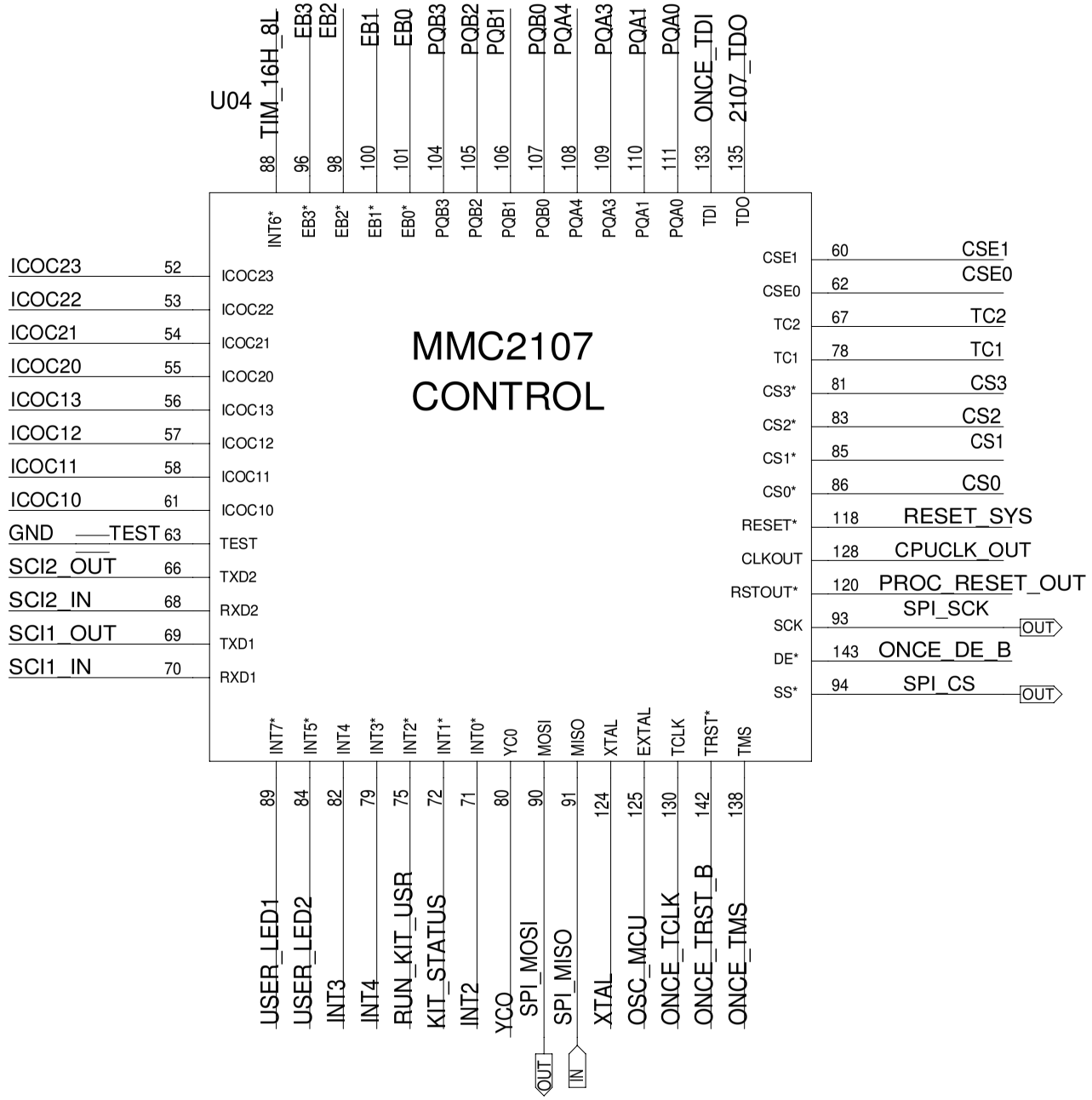
TE3_TSER TE3_TGCLK TE3_TSOFO_TDEN TE3_RSER TE3_RGCLK TE3_RSOFO_RDEN

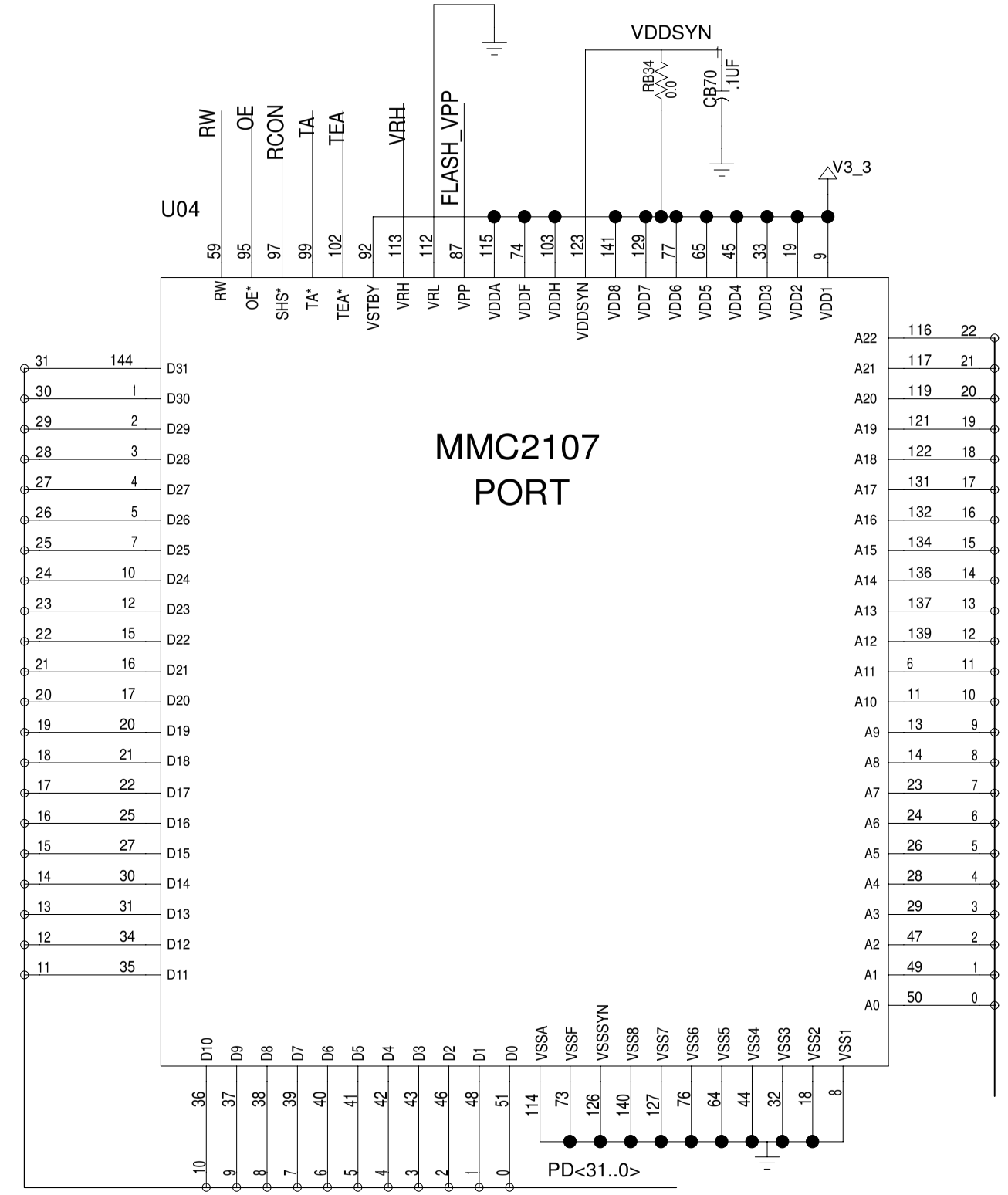
TPB03 TPB04

BEGINNING/END OF T3E3 HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 12/19(TOTAL)

BLOCK NAME: _te3wan_dn. PARENT BLOCK: _ztopdn_\





BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 1/7(BLOCK) 13/19(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ztopdn_\

PRINTED Fri Jun 20 10:02:20 2008

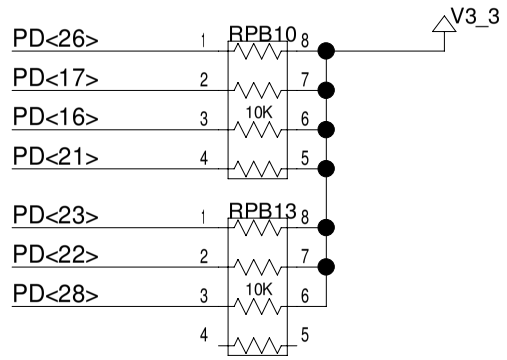
RESET CONFIGURATION

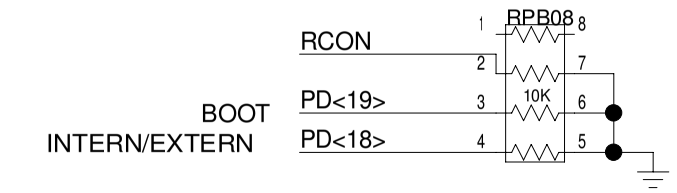
MASTER MODE

FULL DRIVE

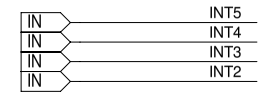
XTAL W/ PLL

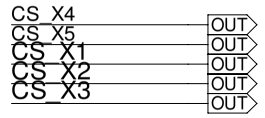
INTERNAL
FLASH ENABLE

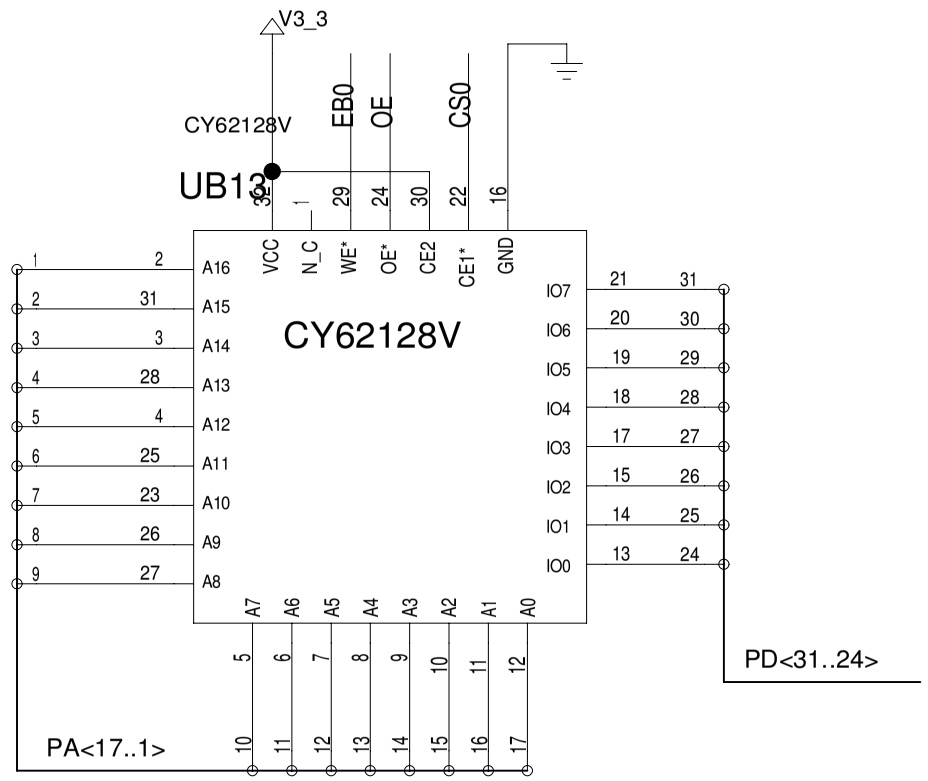


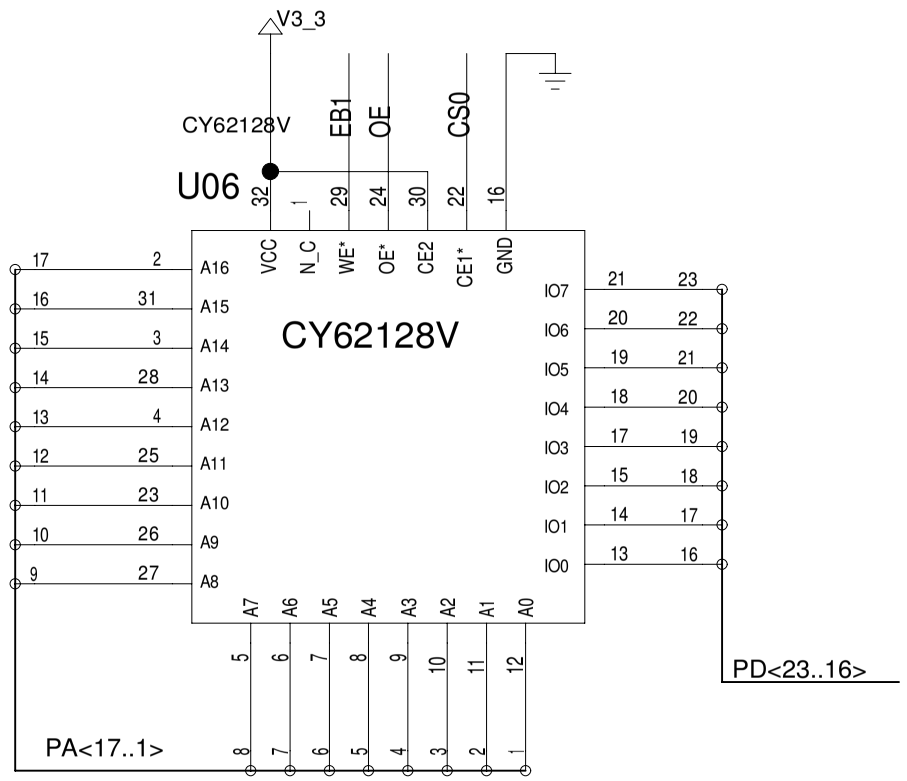


WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND



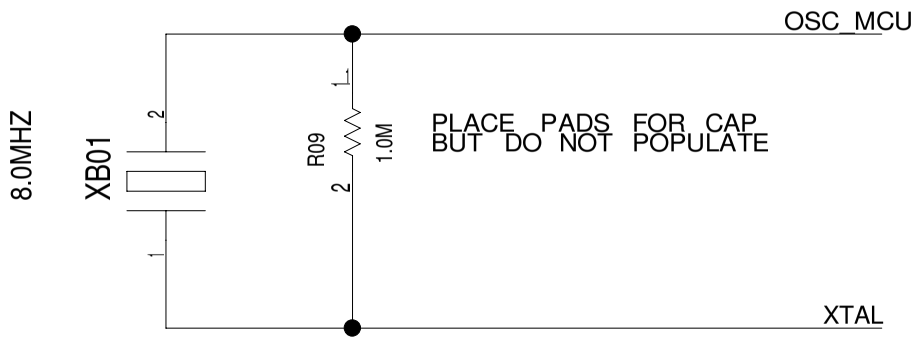


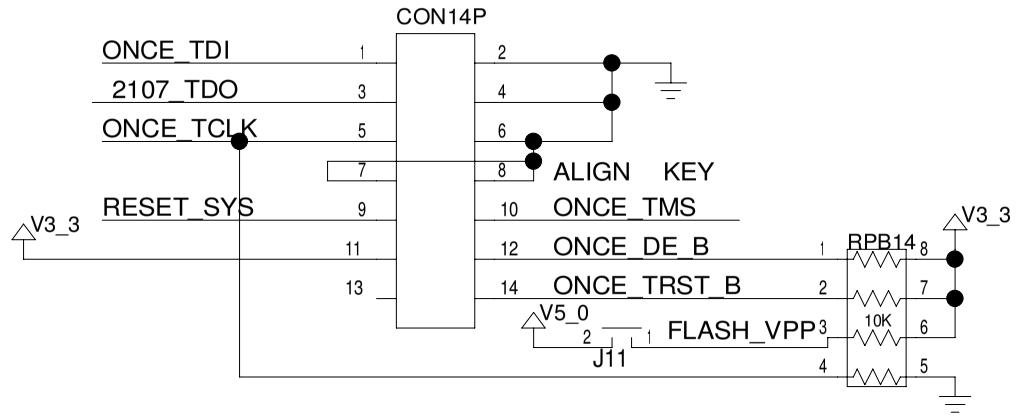


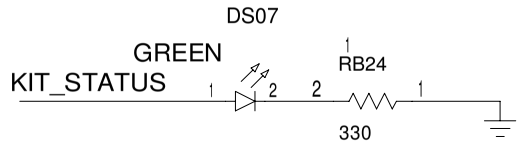


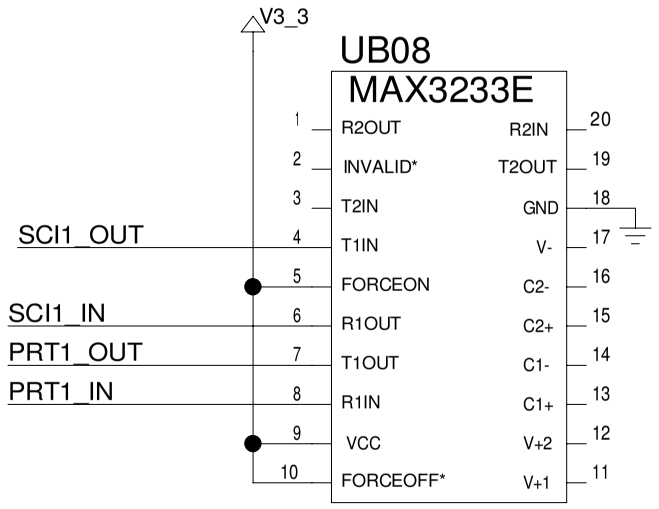
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 2/7(BLOCK) 14/19(TOTAL)

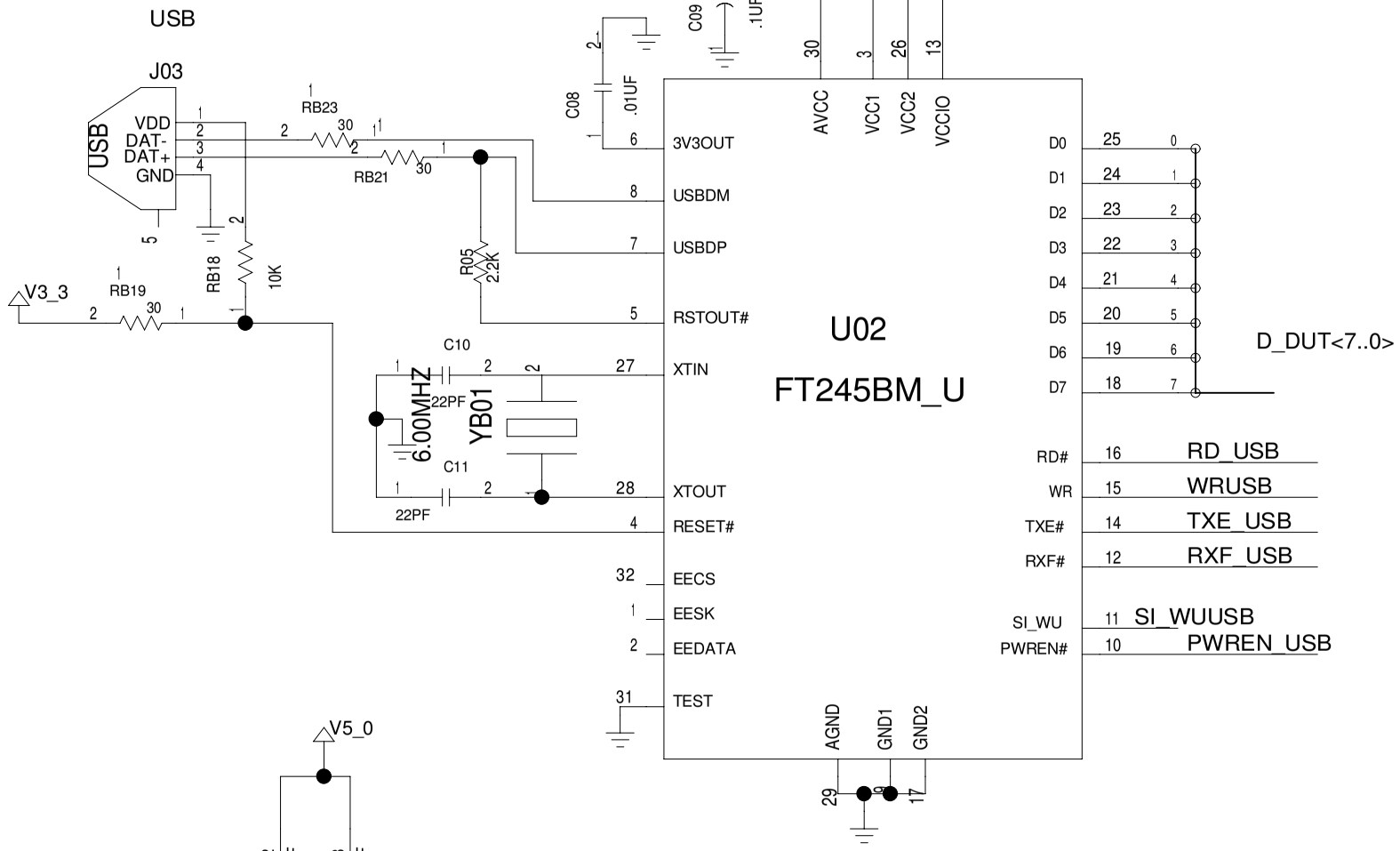
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ztopdn_\

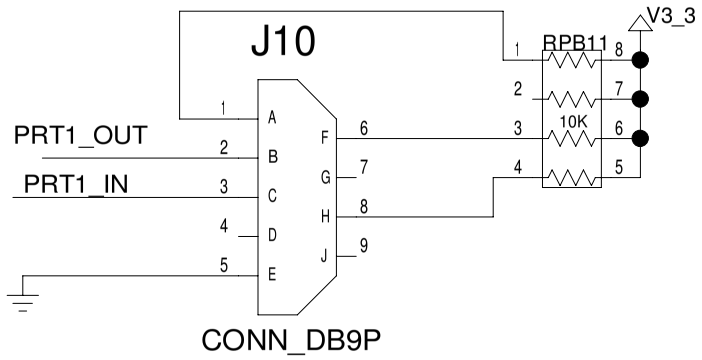


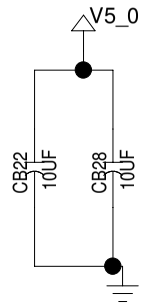






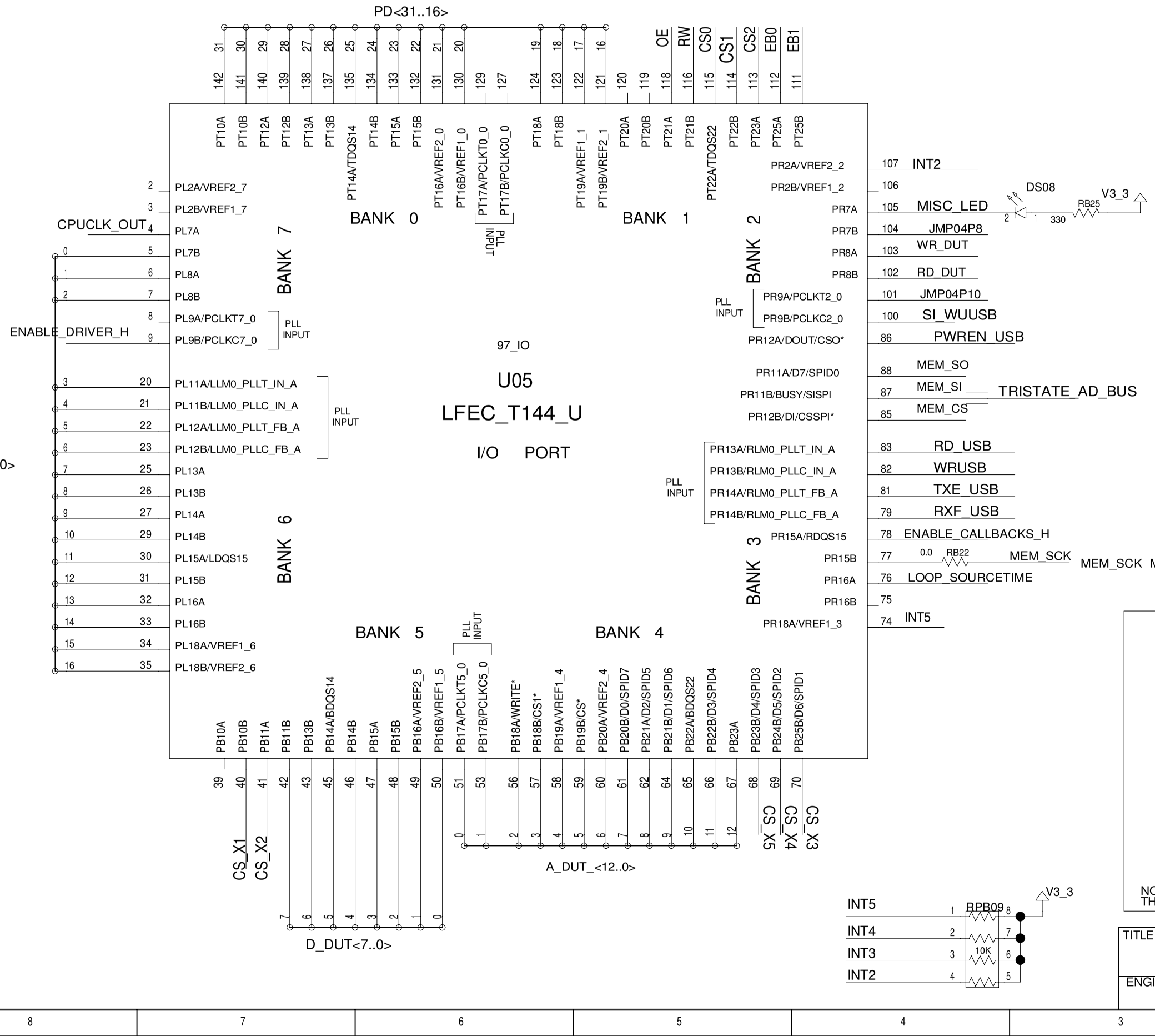


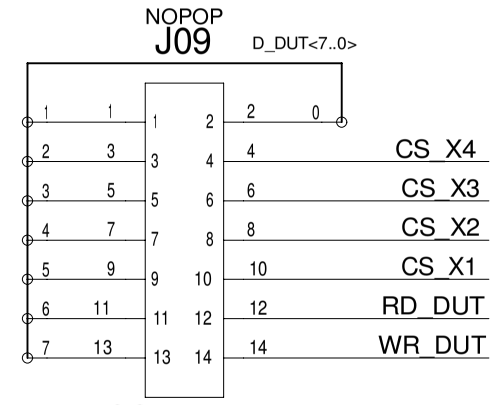


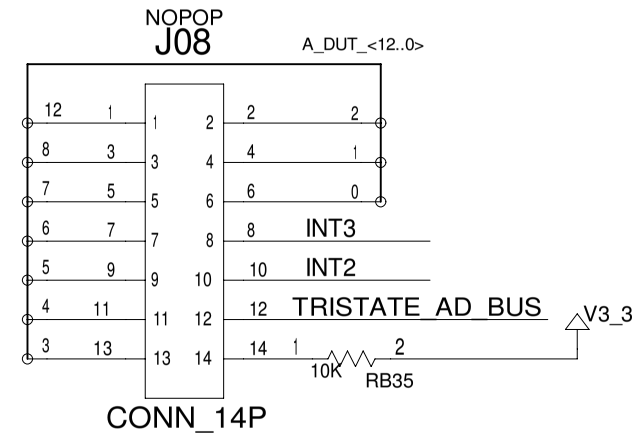


TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 3/7(BLOCK) 15/19(TOTAL)

BLOCK_NAME: motprocrescard_dn. PARENT_BLOCK: \ ztopdn \

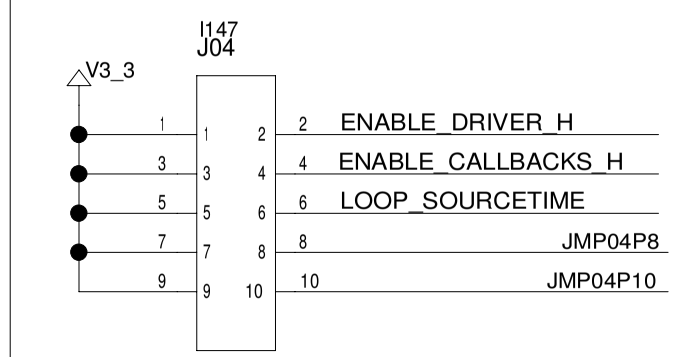






JUMPER PINS 12+14 TO TRISTATE
THE ADDRESS DATABUSS OF THE FPGA.
THIS ALLOWS THE USER TO
CONNECT A DIFFERENT PROCESSOR

MEM_SCK MUST BE AT PIN77 FOR TQFP144

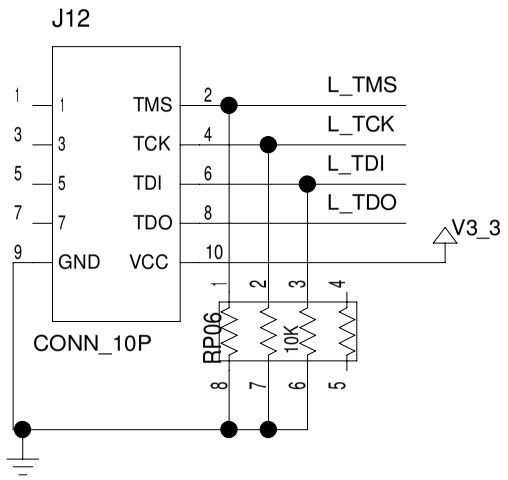


DRIVER / CALLBACKS / LOOPTIME
SIGNALS HAVE PULLDOWNS INSIDE FPGA

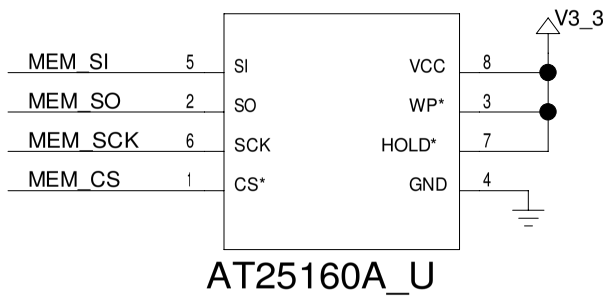
NOTE: J04 PINS 1,3,5,7,9 WERE LEFT UNCONNECTED
THEY ARE NOW CONNECTED TO VCC BY REWORK WIRE

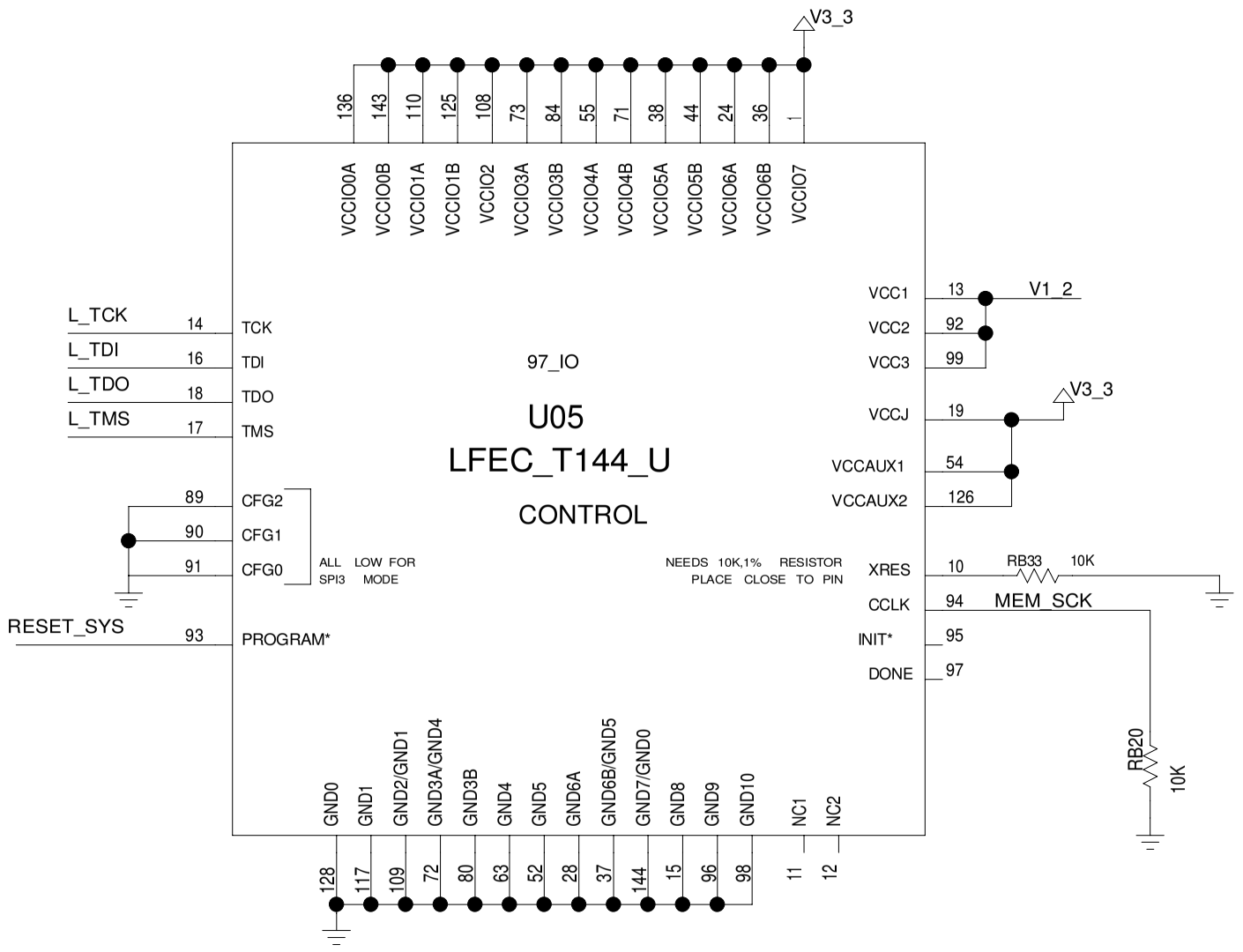
TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 4/7(BLOCK) 16/19(TOTAL)

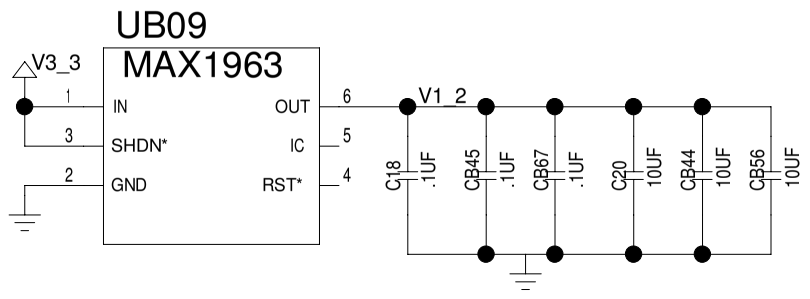
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ztopdn_\



2.7V







TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 5/7(BLOCK) 17/19(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ztopdn_\

J01

2.1MM/5.5MM

V5_0

DB01

L1

5V DC POWER SUPPLY AND
REVERSE BIAS PROTECTION

UB01
MAX1793_U

REGULATOR_INPUT

IN1 IN2 IN3 IN4 RST SHDN

OUT1 OUT2 OUT3 OUT4 SET GND GND

REGULATOR1_OUTPUT

68UF CB02

C07 10UF

3.3V

RB01 0.0

RB02 0.0

SUPPLY_OUTPUT

V3_3

UB04
MAX1793_U

REGULATOR_INPUT

REGULATOR2_OUTPUT

C04 10UF

3.3V

3.3V 1% REGULATOR

UB02
MAX1793_U

REGULATOR_INPUT

REGULATOR3_OUTPUT

68UF CB03

C06 10UF

3.3V

RB03 0.0

RB04 0.0

SUPPLY_OUTPUT

V3_3

UB03
MAX1793_U

REGULATOR_INPUT

REGULATOR4_OUTPUT

C05 10UF

3.3V 1% REGULATOR

TRACES BETWEEN REGULATOR OUTPUT AND V3.3 SHOULD
BE LONG ENOUGH TO BUILD 0.06 OHM OF RESISTANCE
TO ENSURE LOAD SHARING BETWEEN THE 3.3V 1% REGULATORS
TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

3.08V

UB11
MAX811_U

SW01

MR* GND VCC RESET*

V3_3

DS11 GREEN

RPB15

330

RESET_SYS

REGULATOR_INPUT

68UF CB01

68UF CB12

C02 10UF

C03 10UF

C01 10UF

CB73 10UF

GND_TP02
GND_TP04
GND_TPB01
GND_TP03

.50STANDOFF_NUT

H06 H05 H01 H02 H03 H04

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 6/7(BLOCK) 18/19(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ztopdn_\

V3_3

I67 V3_3

I68 GND

V3_3

C33 4.7UF, C32 4.7UF, CB53 4.7UF, CB79 4.7UF, CB77 4.7UF, CB81 4.7UF, CB41 4.7UF, CB76 .1UF, C24 .1UF, CB55 .1UF, CB57 .01UF, CB65 .01UF, CB69 .01UF, CB59 .01UF, C26 4.7UF, C35 4.7UF, C34 4.7UF, CB72 4.7UF, CB30 4.7UF, CB98 4.7UF, C39 .1UF, C38 .1UF, CB34 .1UF, CB27 .01UF, C40 .01UF, C22 .01UF, C37 .01UF, C21 4.7UF, C28 4.7UF, C25 4.7UF, CB100 4.7UF, CB43 4.7UF, CB42 4.7UF, CB37 .1UF, CB96 .1UF, CB93 .1UF, C36 .01UF, CB54 .01UF, CB80 .01UF, CB78 .01UF

V3_3

CB92 4.7UF, CB89 4.7UF, CB38 4.7UF, CB31 4.7UF, CB68 4.7UF, CB66 4.7UF, CB51 4.7UF, CB29 .1UF, CB71 .1UF, CB58 .1UF, CB47 .01UF, CB97 .01UF, CB99 .01UF, C41 .01UF, C47 4.7UF, C43 4.7UF, CB85 4.7UF, C46 4.7UF, CB61 4.7UF, CB83 4.7UF, CB50 .1UF, CB74 .1UF, CB87 .1UF, CB84 .01UF, CB91 .01UF, CB94 .01UF, C42 .01UF, CB24 4.7UF, CB75 4.7UF, C15 4.7UF, CB25 4.7UF, CB62 4.7UF, CB48 4.7UF, C45 .1UF, CB88 .1UF, CB86 .1UF, CB82 .01UF, CB90 .01UF, CB35 .01UF, CB19 .01UF

END OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33Z11DK02A0	DATE: 02/06/2007
ENGINEER: STEVE SCULLY	PAGE: 19/19(TOTAL)